PLESSEY
Semiconductors

TDA2591/3

LINE OSCILLATOR COMBINATION

The TDA2591 and TDA2593 are integrated line oscillator circuits for colour television receivers using thyristor or transistor line deflection output stages.

The circuits incorporate a line oscillator which is based on the threshold switching principle, a line deflection output stage capable of direct drive of thyristor deflection circuits, phase comparison between the oscillator voltage and both the sync pulse and line flyback pulse. Also included on the chip is a switch for changing the filter characteristic and the gate circuit when used for VCR.

The TDA2593 generates a sandcastle pulse (at pin 7) suitable for use with the TDA2532.

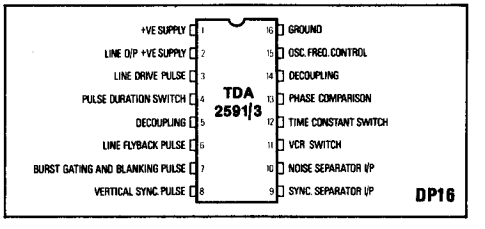

Fig.1 Pin connections (top view)

FEATURES

- Coincidence Detector
- Sync Separator
- Noise Separator
- Vertical Sync Separator
- Colour Burst Keying
- Line Flyback Pulse Generator
- Output Pulse Phase Shifter
- Output Pulse Duration Switching
- Sync Gating Pulse Generator
- Low Supply Voltage Protection

QUICK REFERENCE DATA

- Supply Voltage (pin 1) 12V typ.
- Supply Current 30mA typ.
- Sync Separator Input (pin 9) 3V p-p typ.
- Pulse Duration Switch Input (pin 4)
  at $t = 7\mu s$ 9.4V to V_1
  at $t = 14\mu s + t_d$ 0V to 4V
- VCR Switch ON (pin 11) 0V to 1.5V and 9V to V_1

Output signal

- Vertical Sync Pulse (pin 8) 11V p-p (typ.)
- Burst Gating Pulse (pin 7) 11V p-p (typ.)
- Line Drive Pulse (pin 3) 10.5V p-p (typ.)

ABSOLUTE MAXIMUM RATINGS

Voltages		
Supply pin 1 (when supplied by the IC)	13.2V	
Supply pin 2	18V	
Pin 4	0V to 13.2V	
Pin 9	−6V to +6V	
Pin 10	−6V to +6V	
Pin 11	0V to 13.2V	
Currents		
Pin 2	400mA peak	} 650mA thyristor drive only
Pin 3	400mA peak	
Pin 4	1mA peak	
Pin 6	10mA peak	
Pin 7	10mA peak	
Pin 11	2mA peak	
Power dissipation		
Total power dissipation	800mW	
Temperature		
Storage temperature	−55°C to +125°C	
Operating ambient temperature	−10°C to +60°C	

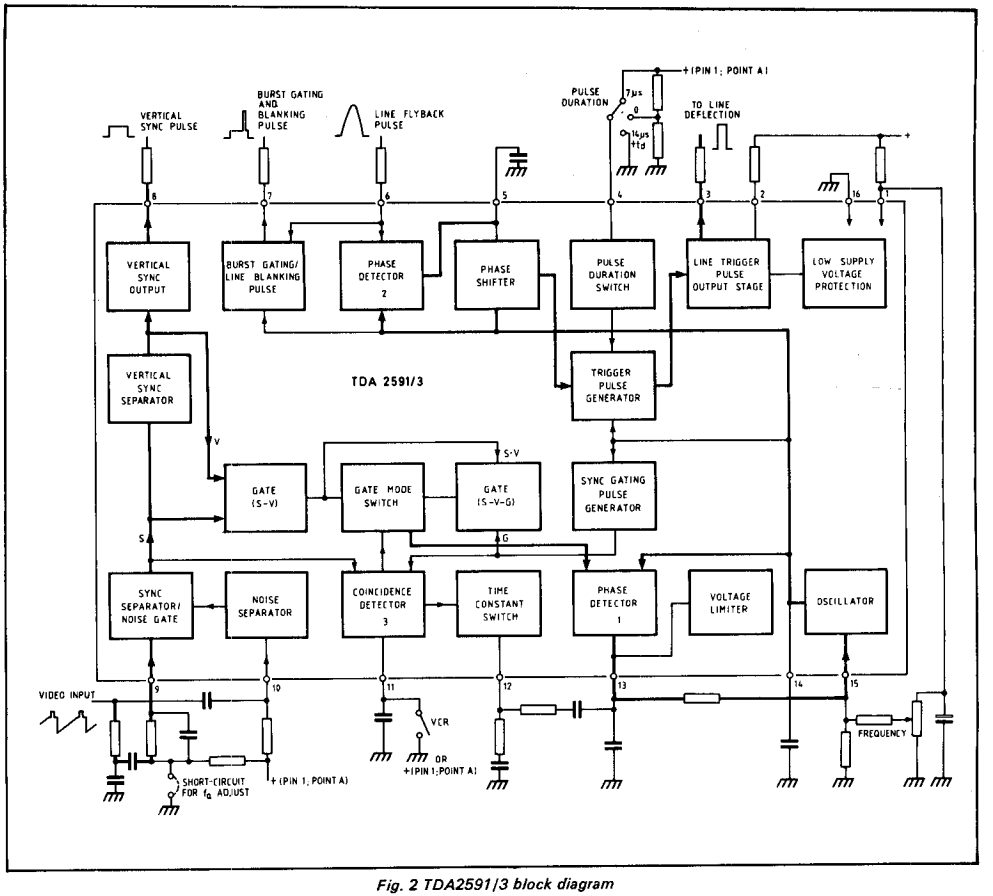

Fig. 2 TDA2591/3 block diagram

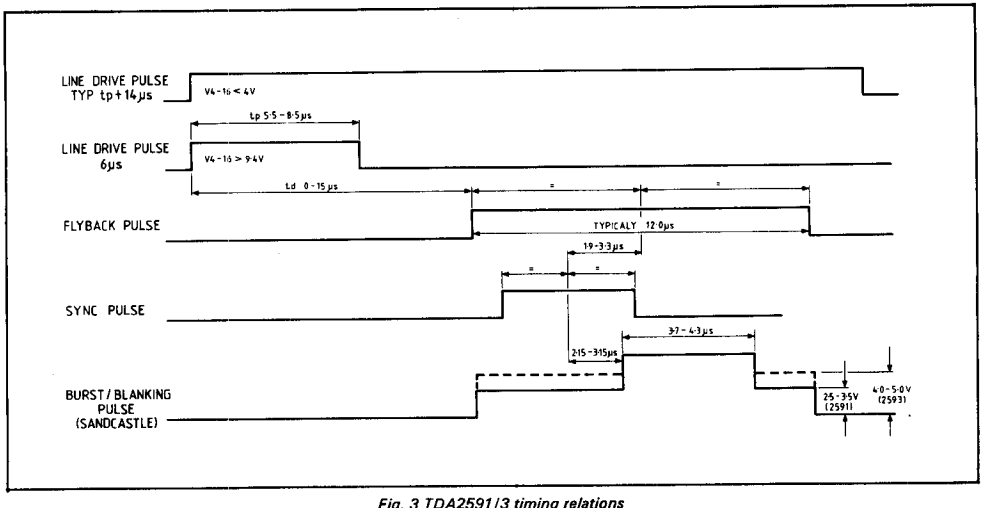

Fig. 3 TDA2591/3 timing relations

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_1 = 12V$
$T_{amb} = +25°C$
Refer to timing diagram, Fig. 3 and Application circuit, Fig. 4
Voltages are referred to pin 6

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Sync separator	9					
Input switching voltage			0.8		V	
Input keying current		5		100	μA	
Input blocking current				1	μA	$V_9 = -5V$
Input switching current				5	μA	
Noise separator	10					
Input switching voltage			1.4		V	
Input keying current		5		100	μA	
Input switching current			150		μA	
Input blocking current				1	μA	$V_{10} = -5V$
Line flyback pulse	6					
Input current		10			μA	
Input switching voltage			1.4		V	
Input limiting voltage		−0.7		+1.4	V	
Input resistance			400		Ω	
Pulse duration switch	4					
Input voltage		9.4		V_1	V	$t = 7\mu s$
Input current		200			μA	
Input voltage		0		4.0	V	$t = 14\mu s + t_d$
Input current		200			μA	
Input voltage		5.4		6.5	V	$t = 0, V_3 = 0$
Input current (input open)			0		μA	See note 1
VCR Switching	11					
Input voltage (typical range)		0		1.5	V	See note 2
		9		V_1	V	
Input current		200			μA	$V_{11} = 0V$ to 1.5V
Output current		1		2	mA	$V_{11} = 9V$ to V_1
Vertical sync pulse (positive going)	8					
Output voltage		10	11		Vp–p	
Output resistance			2		kΩ	
Burst gating pulse (positive-going)	7					
Output voltage		10	11		Vp–p	
Output resistance			400		Ω	
Blanking pulse	7					
Output voltage (typical range) 2591		2.5		3.5	Vp–p	
Output voltage (typical range) 2593		4.0		5.0	Vp–p	
Output resistance			400		Ω	
Line drive pulse (positive going)	3					
Output voltage			10.5		Vp–p	
Output current (average value)			100		mA	
Output resistance for leading edge of line pulse			2.5		Ω	
Output resistance for trailing edge of line pulse			20		Ω	
Oscillator	14					
Threshold voltage low level			4.4		V	
Threshold voltage high level			7.6		V	
Discharge current			0.47		mA	
Phase comparison (ϕ_1: sync pulse/oscillator)	13					
Control voltage range (typ)		3.8		8.2	V	
Control current		1.9	2.1	2.3	mAp–p	
Output blocking current				1	μA	$V_{13} = 4V$ to 8V
Output resistance		High (see note 3)				$V_{13} = 4V$ to 8V
		Low (see note 4)				$V_{13} < 3.8V$ or $> 8.2V$
Time constant switch	12					
Output voltage			6		V	
Output current				1	mA	
Output resistance			100		Ω	$V_{11} = 2.5V$ to 7V
			60		kΩ	$V_{11} < 1.5V$ or $> 9V$

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Coincidence detector (ϕ_3)	11					
Output voltage typical range		0.5		6	V	
Output current:						
without coincidence			0.1		mAp–p	
with coincidence			0.5		mAp–p	
Phase comparison (ϕ_2: oscillator/ line flyback pulse)	5					
Control voltage range (typ)		5.4		7.6	V	
Control current			1		mAp–p	
Output resistance		High (see note 3)				$V_5 = 5.4V$ to $7.6V$
			8		kΩ	$V_5 < 5.4V$ or $> 7.6V$
Input current at blocked phase detector				5	μA	$V_5 = 5.4V$ to $7.6V$
Applications (see Fig. 4)	9					
Sync separator						
Input voltage (negative video signal)		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Noise gating	10					
Input voltage		1	3	7	Vp–p	
Input keying current range		5		100	μA	
Superimposed noise voltage				7	Vp–p	
Vertical sync pulse separator						
Delay between leading edge of input and output signal, t_{on}			12		μs	
Delay between trailing edge of input and output signal, t_{off}				t_{on}	μs	
Output voltage	8		11		Vp–p	
Output resistance	8		2		kΩ	
Oscillator						
Frequency: free running			15.625		kHz	$C_{14} = 4.7nF$, $R_{15} = 10k\Omega$
Spread of frequency, $\Delta f_o/f_o$				±5	%	See note 5
Frequency control sensitivity, $\Delta f_o/\Delta I_{15}$			31		Hz/μA	
Adjustment range of network in Fig. 2			±10		%	
Influence of supply voltage on frequency $\frac{\Delta f_c/f_o}{\Delta V/V_{nom}}$				±0.05		See note 5, $V_1 = 12V$
Change of frequency when V_1 drops to 5V				±10	%	See note 5
Temperature coefficient of oscillator frequency per °C				$\pm 10^{-4}$		
Phase comparison (ϕ_1: sync pulse/oscillator)						
Control sensitivity			2		kHz/μs	
Catching and holding range (82kΩ between pins 13 and 15)			±780		Hz	$R_{13-15} = 82k\Omega$
Spread of catching and holding range			±10		%	See note 5
Phase comparison (ϕ_2: oscillator/ line flyback pulse)						
Permissible delay between leading edge of output pulse and leading edge of flyback pulse, Δtd		0		15	μs	
Static control error, td/td				0.2	%	
Overall phase relation See Note 6						
Phase relation between middle of sync pulse and the middle of the flyback pulse, t			2.6		μs	
Tolerance of phase relation Δt				0.7	μs	
Adjustment sensitivity of overall phase relation	5					
caused by: adjustment voltage $\Delta V_5/\Delta t$			0.1		V/μs	
adjustment current, $\Delta I_5/\Delta t$			30		μA/μs	

ELECTRICAL CHARACTERISTICS (Contd.)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Burst gating pulse						
Pulse width	7	3.7	4.0	4.3	µs	At 7V level
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse	7	2.15	2.65	3.15	µs	$V_7 = 7V$ At 7V level
Line drive pulse						
Output pulse duration, t_p	3	5.5	7.0	8.5	µs	$V_4 > 9.4V$
	3		$14 + t_d$		µs	$V_4 < 4V$, see note 7
Supply voltage for switching off the output pulse	1		4		V	
Internal gating pulse						
Pulse duration			7.5		µs	

NOTES
1. May also be left unconnected
2. VCR 'on' is normally achieved by connecting pins 11, via the VCR switch, to either ground or V_1
3. Current source
4. Emitter follower
5. Excluding external component tolerances
6. The adjustment of the overall phase relation and consequently the leading edge of the output pulse occurs automatically by phase detector 2 (See Fig. 2)
7. t_d = switch-off delay of line output stage.

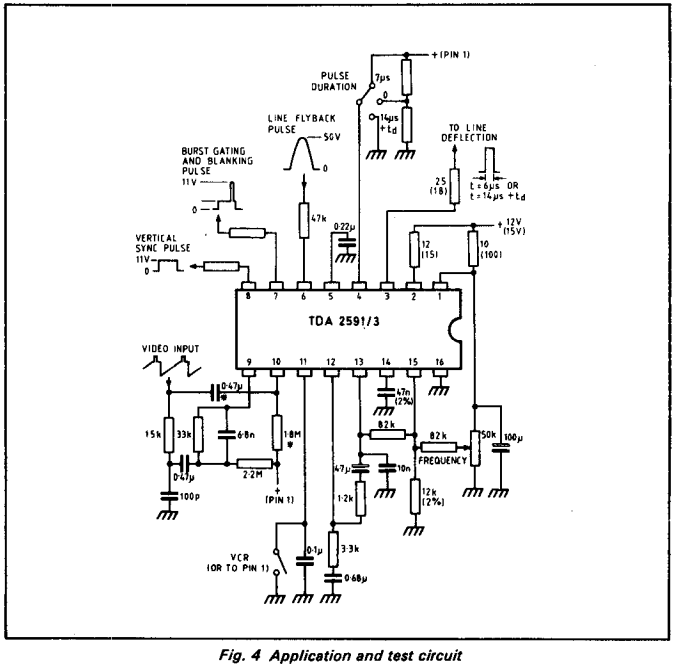

Fig. 4 Application and test circuit