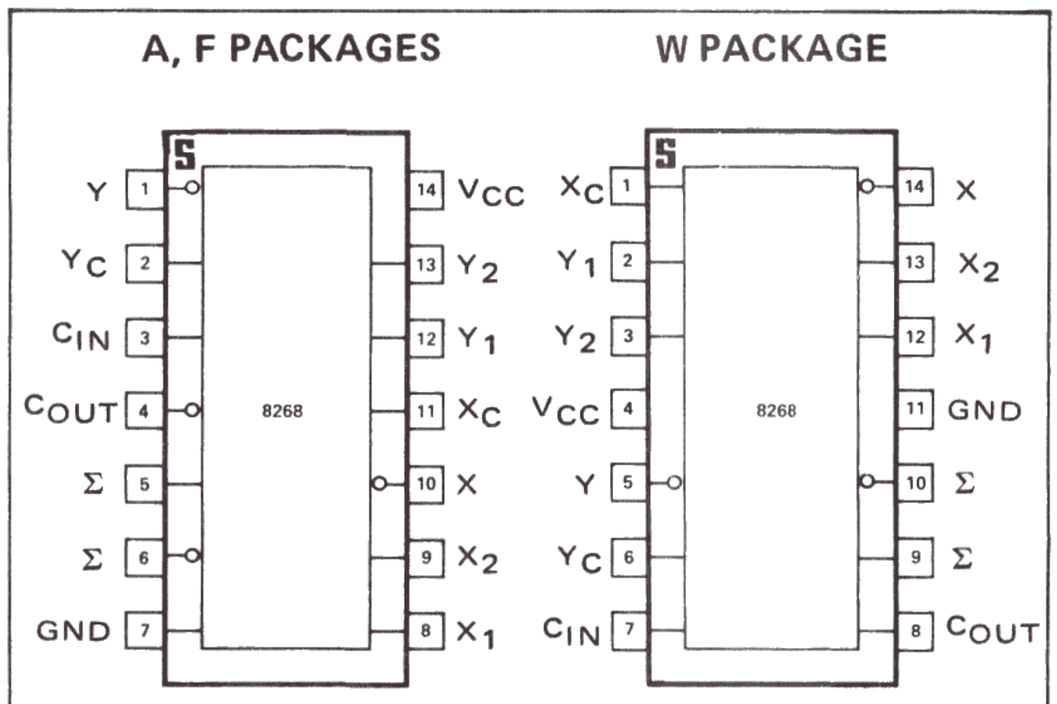
DESCRIPTION

The 8268 is a single-bit full adder with gated true and complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and an inverted carry output. By taking advantage of the unique true or inverted inputs and true or inverted outputs, parallel addition speed is greatly enhanced (by eliminating unnecessary inversions).

The device is designed for medium speed parallel and serial adder systems.

PIN CONFIGURATIONS (Top View)



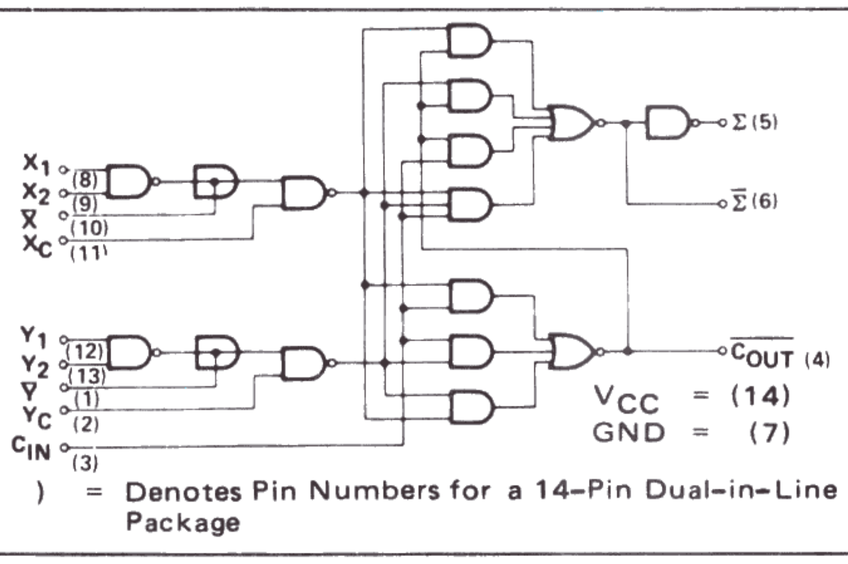
TRUTH TABLE (See Notes 1, 2 and 3)

C_{IN}	Y	X	$\overline{C_{OUT}}$	Σ	$\overline{\Sigma}$
0	0	0	1	0	1
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	1	0

NOTES:

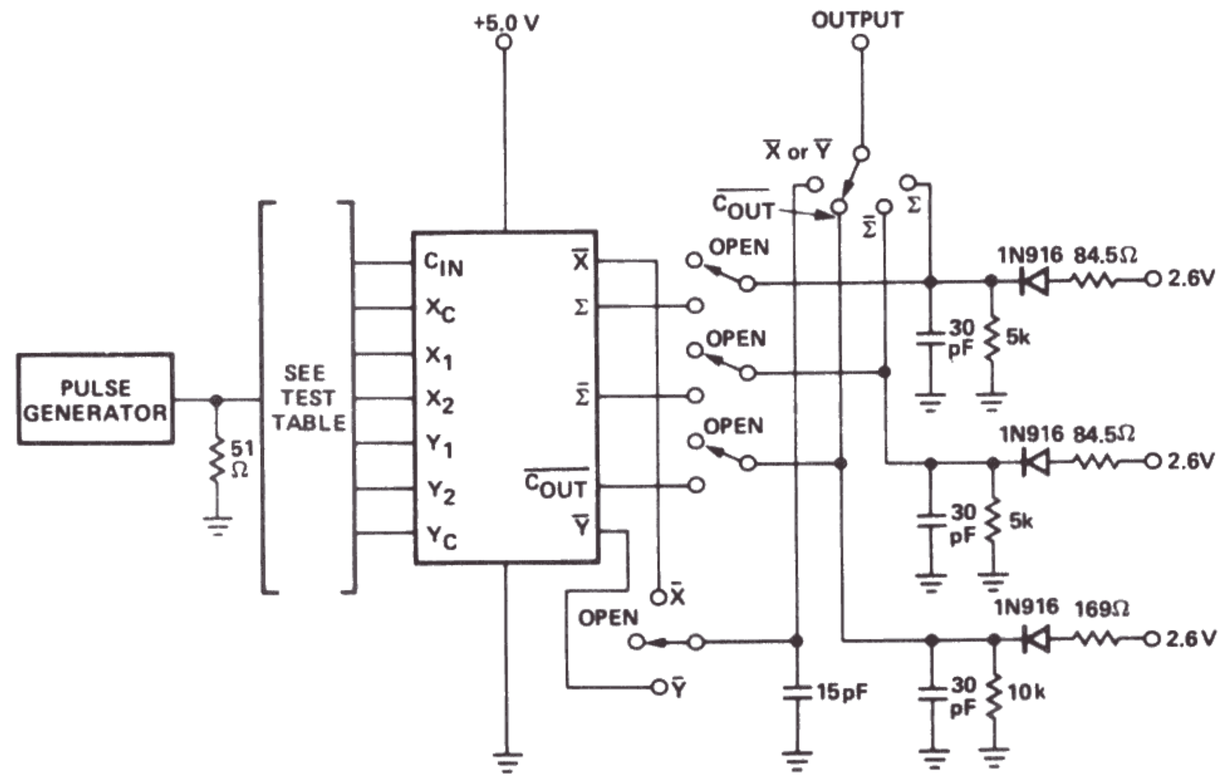
1. $X = \overline{\overline{X} \cdot X_C}$; $Y = \overline{\overline{Y} \cdot Y_C}$
   where $\overline{X} = \overline{X_1 \cdot Y_2}$; $\overline{Y} = \overline{Y_1 \cdot Y_2}$
2. When $\overline{X}$ or $\overline{Y}$ are used as inputs, X_1 and X_2 or Y_1 and Y_2 respectively must be tied to GND.
3. When X_1 and X_2 or Y_1 and Y_2 are used as inputs, $\overline{X}$ or $\overline{Y}$ respectively must be left open or used to perform the WIRED-AND function.

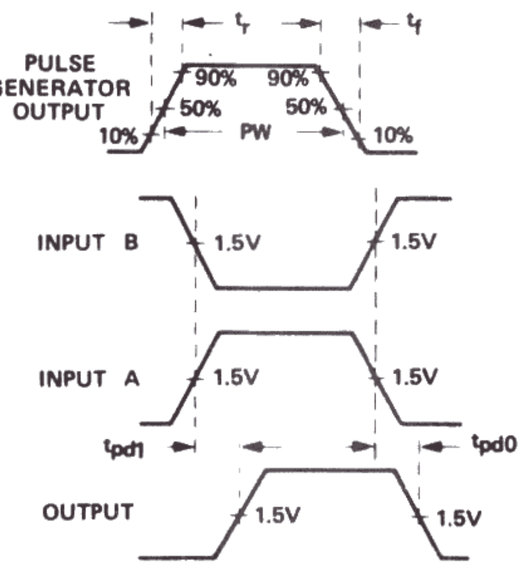
LOGIC DIAGRAM



( ) = Denotes Pin Numbers for a 14-Pin Dual-in-Line Package

AC TEST FIGURE AND WAVE FORMS





NOTES

1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics:
   V_{gen} = 2.6V, tr = tf $\leqslant$ 15ns. PW = 0.5ns, PRR = 1MHz.
5. Inputs and outputs not otherwise specified are open.
6. Capacitance shown include probe and jig capacitance.
7. All resistances are in ohms.

ELECTRICAL CHARACTERISTICS Over Recommended Operating Temperature And Voltage

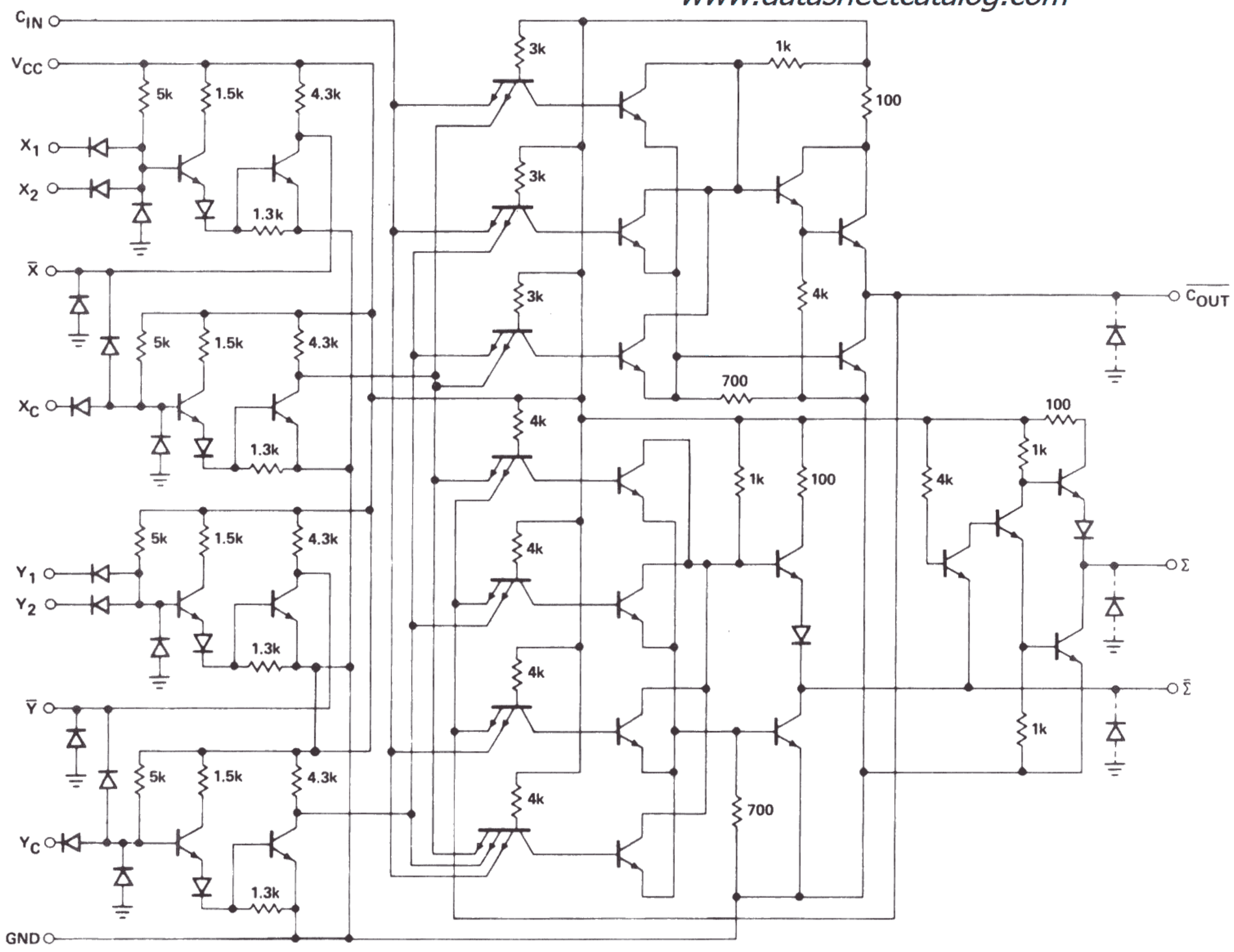
CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
"1" Output Voltage	2.6	3.5		V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	0.8V	2.0V	0.8V	-500μA	6
"0" Output Voltage			0.4	V	0.8V	0.8V	2.0V	2.0V	0.8V	0.8V	2.0V	2.0V	0.8V	16mA	7
"0" Input Current															
X_1	-0.1		-1.6	mA	0.4V	4.5V									
X_2	-0.1		-1.6	mA	4.5V	0.4V									
X	-0.1		-2.6	mA	0.0V	0.0V	0.4V	4.5V							
X_c	-0.1		-1.6	mA	0.0V	0.0V		0.4V							
Y_1	-0.1		-1.6	mA					0.4V	4.5V					
Y_2	-0.1		-1.6	mA					4.5V	0.4V					
Y	-0.1		-2.6	mA					0.0V	0.0V	0.4V	4.5V			
Y_c	-0.1		-1.6	mA					0.0V	0.0V		0.4V			
C_{IN}	-0.1		-8.0	mA									0.4V		
"1" Input Current															
X_1			40	μA	4.5V										
X_2			40	μA	0.0V										
X_c			40	μA			0.0V	4.5V							
Y_1			40	μA					4.5V	4.5V					
Y_2			40	μA					0.0V	0.4V					
Y_c			40	μA							0.0V	4.5V			
C_{IN}			160	μA	0.0V	0.0V			0.0V	0.0V			4.5V		
Input Voltage Rating															12
X_1	5.5			V	10mA	0.0V									
X_2	5.5			V	0.0V	10mA									
X_c	5.5			V			0.0V	10mA							
Y_1	5.5			V					10mA	0.0V					
Y_2	5.5			V					0.0V	10mA					
Y_c	5.5			V							0.0V	10mA			
C_{IN}	5.5			V									10mA		

$T_A = 25°C$ and $V_{CC} = 5.0V$

CHARACTERISTICS	LIMITS				TEST CONDITIONS										NOTES
	MIN.	TYP.	MAX.	UNITS	X_1	X_2	X	X_c	Y_1	Y_2	Y	Y_c	C_{IN}	OUTPUTS	
Power/Current Consumption		152/ 29	185/ 35	mW/ mA											11
Output Short Circuit Current (Σ)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V	0.0V		2.0V	0.0V	10, 11
Output Short Circuit Current ($\overline{\Sigma}$)	-18		-57	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	10, 11
Output Short Circuit Current ($\overline{C}_{out}$)	-18		-70	mA	0.0V	0.0V			0.0V	0.0V			0.0V	0.0V	10, 11
t_{pd} 1 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 0 C_{in} to $\overline{C}_{out}$		8	13	ns											8
t_{pd} 1 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 0 Y_c to $\overline{C}_{out}$		20	25	ns											8
t_{pd} 1 X_c to Σ		35	45	ns											8
t_{pd} 0 X_c to Σ		35	45	ns											8
t_{pd} 1 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} 0 Y_c to $\overline{\Sigma}$		25	35	ns											8
t_{pd} X_1, X_2 to $\overline{X}$		30	40	ns											8, 9
t_{pd} 0 X_1, X_2, to $\overline{X}$		15	20	ns											8, 9
t_{pd} 1 Y_1, Y_2, to $\overline{Y}$		30	40	ns											8, 9
t_{pd} 0 Y_1, Y_2, to $\overline{Y}$		15	20	ns											8, 9

NOTES
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition: "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}
8. Refer to AC Test Figure.
9. This test is a measure of the required worst-case data set-up time.
10. Not more than one output should be shorted at a time.
11. V_{CC}=5.25 volts.
12. The total time required to perform the ADD function may be determined by summing the delays from X_1, X_2 to $\overline{X}$ or Y, Y_2 to $\overline{Y}$ with the delay from X_C or Y_C to Σ or $\overline{\Sigma}$.

SCHEMATIC DIAGRAM

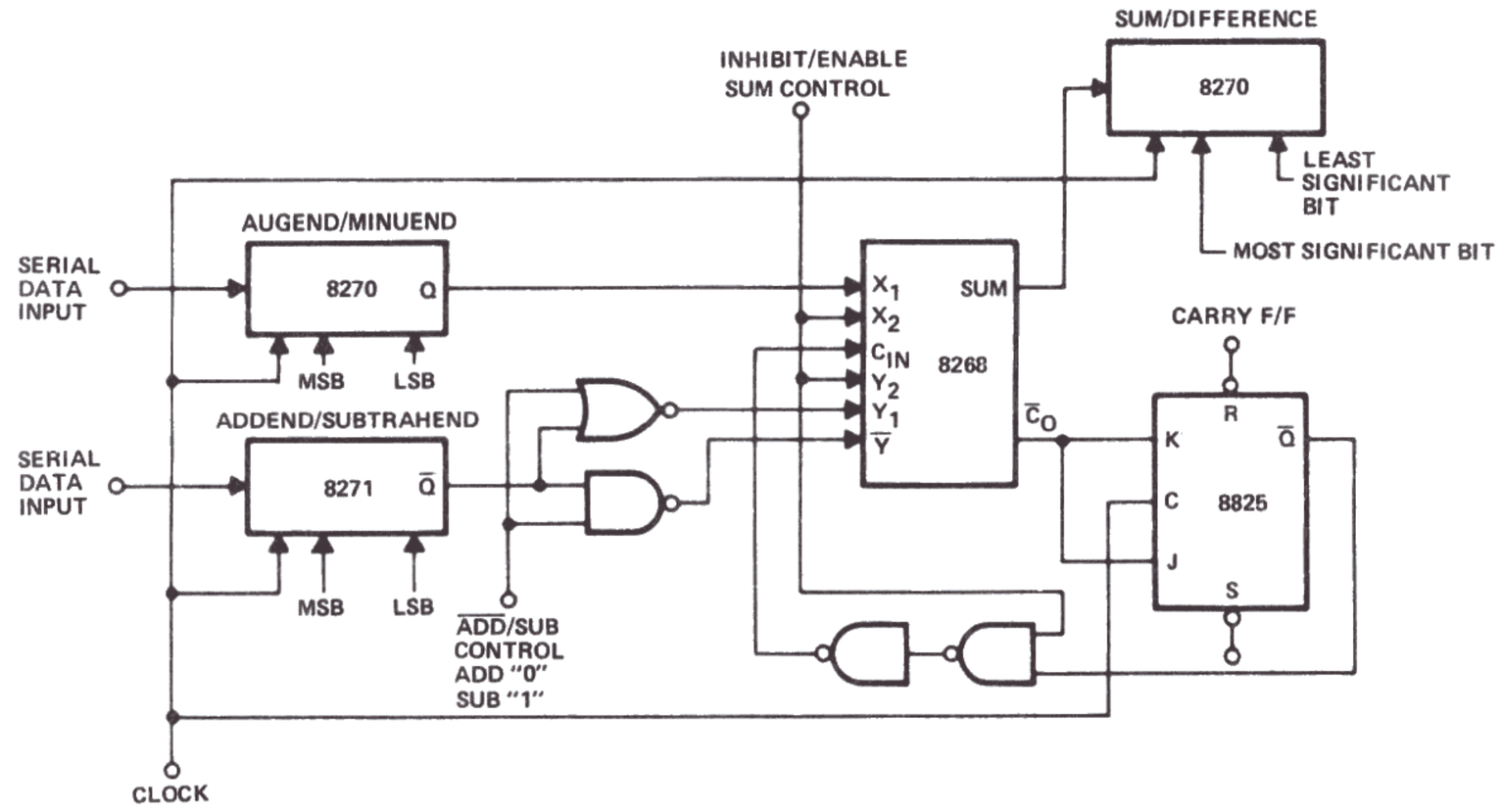


TEST TABLE (See Note 5)

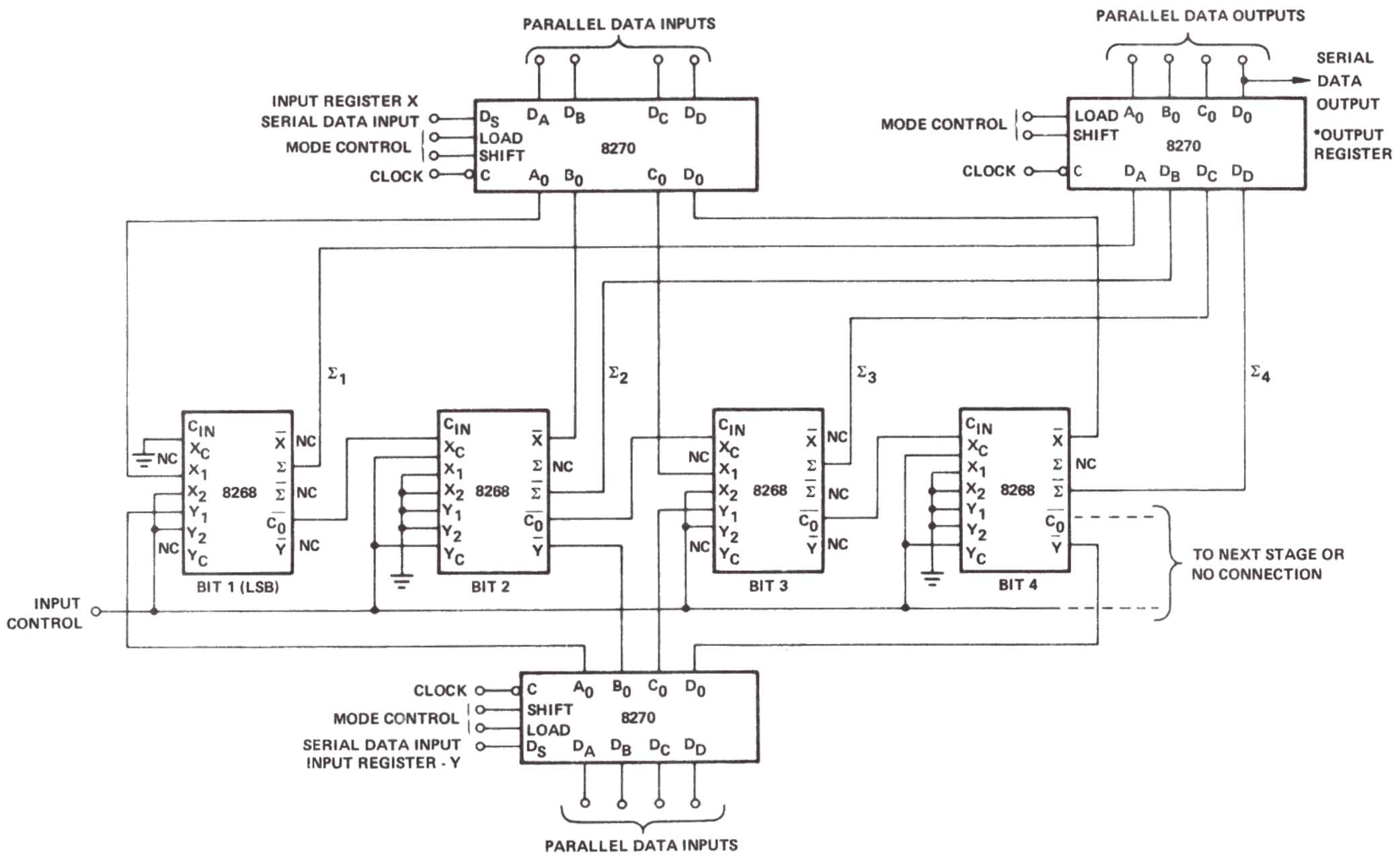
TEST NO.	OUTPUTS UNDER TEST	APPLY INPUT A TO	APPLY INPUT B TO	APPLY +2.6V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
2	$\overline{C}_{out}$	None	C_{in}	None	Y_1	$\overline{C}_{out}$
3	$\overline{C}_{out}$	Y_c	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
4	$\overline{C}_{out}$	Y_c	None	C_{in}	X_1, Y_1	$\overline{C}_{out}$
5	Σ	X_c	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
6	Σ	X_c	None	C_{in}	X_1, Y_1	Σ $\overline{\Sigma}$ $\overline{C}_{out}$
7	$\overline{\Sigma}$	Y_c	None	C_{in}	Y_1	$\overline{\Sigma}$
8	$\overline{\Sigma}$	Y_c	None	C_{in}	Y_1	$\overline{\Sigma}$
9	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
10	$\overline{X}$	None	X_1	X_2	None	$\overline{X}$ (CL = 15 pF)
11	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)
12	$\overline{Y}$	None	Y_1	Y_2	None	$\overline{Y}$ (CL = 15 pF)

TYPICAL APPLICATIONS

4-BIT SERIAL ADD/SUBTRACTOR



N-BIT PARALLEL ADDER



NOTES
To expand storage register for serial/parallel operation, connect D_0 to D_s of next stage and common the mode control lines and the clock line of the first stage to their respective second stage equivalents.

*NOTE
To expand output register for parallel outputs common clock, shift and load lines with their respective counterparts. For serial data output, also connect D_0 of first register to D_s of next register.

INTRODUCTION

The 8200 Series MSI, 82S Schottky MSI and 8T interface circuits are described in this section. These devices are directly compatible with other TTL circuits such as the bipolar memories covered in Section 4 and the 54/74 series described in Section 2.

Other 8000 Series circuits such as gates, binaries and several interface elements are described in a separate publication, that may be obtained from your nearest Signetics representative.

The electrical specifications given for the IC's in this section are designed to serve as an exact guide for procurement documents. Detailed test conditions and test limits are given for each integrated circuit. Whenever possible, worst case limits for the electrical parameters have been provided.

Ordering information for the circuits described in this section can be found below. This information should be reviewed in conjunction with detailed package descriptions given in Section 8 where physical dimensions as well as thermal impedance data are given.

Reliability information that details production screens, acceptance tests and qualification tests is given in Section 8 as well. The users attention is also directed to the optional high reliability programs described in Section 8. These are the Signetics SUPR DIP Program for plastic packages and the Signetics SURE 883 program.

Usage information may be found in the Signetics Applications Handbook also available. Additional applications information may be obtained from the nearest Signetics representative or local Signetics field applications engineer. The user may also find the general systems design considerations helpful which are given on pages 3-2 through 3-7.

ORDERING INFORMATION

Unless otherwise specified all devices are available in the "S" and "N" temperature ranges:

"S" = −55°C to +125°C
"N" = 0°C to + 75°C

The package type designators below, in conjunction with detailed package information given in section 8, may be used for procurement purposes.

PART IDENTIFICATION
Y8XXXZ

Y	=	Operating Temperature Range
"S"	=	−55°C to +125°C (Military)
"N"	=	0°C to + 75°C (Commercial)

NOTE: 82XX = Standard MSI
82SXX = Schottky MSI
8TXX = Interface Circuit

Z	=	Package Type Designator
V	=	8-pin Dual-in-line Plastic Package
A	=	14-pin Dual-in-line Plastic Package
B	=	16-pin Dual-in-line Plastic Package
N	=	24-pin Dual-in-line Plastic Package
F	=	14, 16, 24-pin Dual-in-line Ceramic Package (Cerdip)
W	=	14, 16-pin Ceramic Flat Package (Cerpac)
I	=	14, 16, 24-pin Ceramic Dual-in-line Package
Q	=	14, 16, 24-pin Ceramic Flat Package