

4096-BIT (1024-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

This is a 1024-word by 4-bit static RAM fabricated with the silicon-gate CMOS process and designed for low power dissipation and easy application of battery back-up.

While maintained in the chip non-select state by the chip-select signal $\overline{CS}$, it consumes power only at the low value of $15\mu A$ (max) standby current and accordingly is especially suitable as a memory system for battery-operated applications and for battery back-up.

It operates on a single 5V supply, as does TTL, and inputs and outputs are directly TTL-compatible and are provided with common I/O terminals.

FEATURES

- Access time: **450ns (max)**
- Low power dissipation in the standby mode: **$15\mu A$ (max)**
- Single 5V power supply
- Data holding at 2V supply voltage
- No external clock or refreshing operation required
- Both inputs and outputs are directly TTL-compatible
- Outputs are three-state, with OR-tie capability
- Simple memory expansion by chip-select signal
- Data terminals are common for both inputs and outputs
- Pin configuration is identical with that of Mitsubishi's M5L 2114LP N-channel 4K static RAM, Intel's 2114, and TI's TMS4045

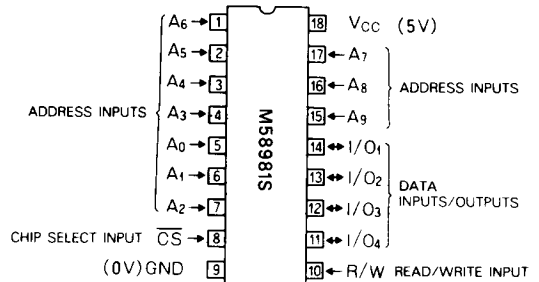
APPLICATION

- Battery-driven or battery back-up small-capacity memory units

FUNCTION

This device provides common data input and output terminals.

PIN CONFIGURATION (TOP VIEW)



Outline 18S1

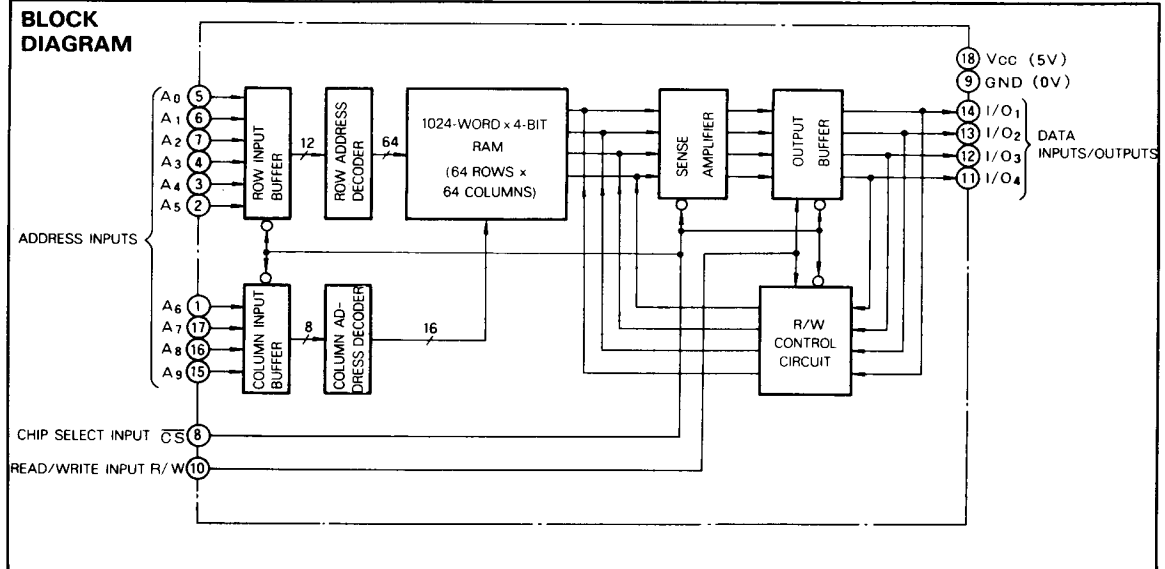
During a write cycle, when a location is designated by address signals $A_0 \sim A_9$ and signal R/W goes low, the data of the I/O at that time is written.

During a read cycle, when a location is designated by address signals $A_0 \sim A_9$, and signal R/W goes high, the data of the designated address is available at the I/O terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance state) useful for OR-ties with the output terminals of other chips.

Also in the chip non-select state, the device operates with a low power dissipation, having a standby current of $15\mu A$ (max), so that the memory data can be held at a supply voltage of 2V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	$-0.3 \sim 7$	V
V_I	Input voltage		$-0.3 \sim V_{CC} + 0.3$	V
V_O	Output voltage		$0 \sim V_{CC}$	V
P_d	Maximum power dissipation	$T_a = 25^\circ\text{C}$	1000	mW
T_{opr}	Operating free-air ambient temperature range		$0 \sim 70$	$^\circ\text{C}$
T_{stg}	Storage temperature range		$-65 \sim 150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-0.3		0.65	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		-0.3		0.65	V
V_{OH}	High-level output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim 5.5\text{V}$			± 1	μA
I_{OZH}	Off-state high-level output current	$V_I(\overline{CS}) = 2.2\text{V}$, $V_O = 2.4\text{V} \sim V_{CC}$			1	μA
I_{OZL}	Off-state low-level output current	$V_I(\overline{CS}) = 2.2\text{V}$, $V_O = 0.4\text{V}$			-1	μA
I_{CC1}	Supply current from V_{CC}	$\overline{CS} \leq 0.01\text{V}$, other inputs = V_{CC} , Output open		9	25	mA
I_{CC2}	Supply current from V_{CC}	$\overline{CS} \leq 0.01\text{V}$, other inputs = 2.2V , Output open		13	30	mA
I_{CC3}	Supply current from V_{CC}	$V_I(\overline{CS}) = V_{CC}$			15	μA
C_I	Input capacitance, all inputs	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$		4	8	pF
C_O	Output capacitance	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$		8	12	pF

Note 1: Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	Input pulse	450			ns
$t_{su(AD)}$	Address setup time with respect to write pulse	$V_{IH} = 2.2\text{V}$	130			ns
$t_{w(WR)}$	Write pulse width	$V_{OH} = 0.65\text{V}$	250			ns
t_{wr}	Write recovery time	$t_r = t_f = 20\text{ns}$	50			ns
$t_{su(DA)}$	Data setup time	Reference level = 1.5V	250			ns
$t_h(DA)$	Data hold time	Load = 1TTTL , $C_L = 100\text{pF}$	0			ns
$t_{su}(\overline{CS})$	Chip select setup time		350			ns
$t_{pxz(WR)}$	Output disable time with respect to write pulse				100	ns

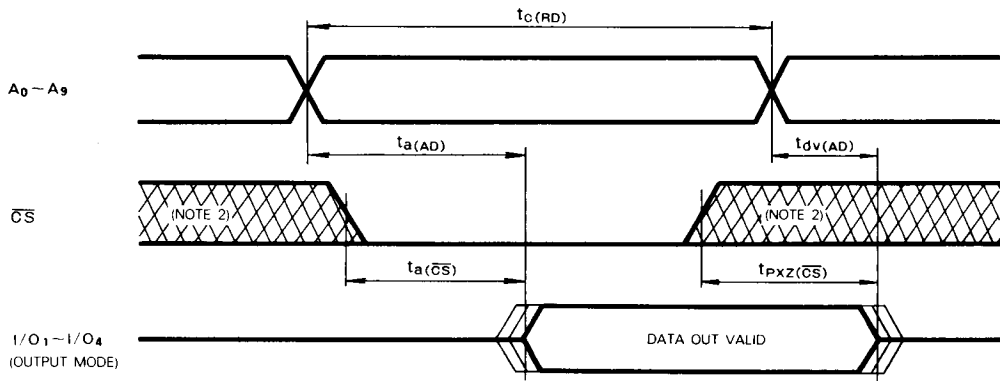
SWITCHING CHARACTERISTICS (For Read Cycle) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	Input pulse	450			ns
$t_a(AD)$	Address access time	$V_{IH} = 2.2\text{V}$, $V_{OH} = 0.6\text{V}$			450	ns
$t_a(\overline{CS})$	Chip select access time	$t_r = t_f = 20\text{ns}$			450	ns
$t_{pxz}(\overline{CS})$	Output disable time with respect to chip select	Reference level = 1.5V Load = 1TTTL , $C_L = 100\text{pF}$			130	ns
$t_{dv(AD)}$	Data valid time with respect to address		0			ns

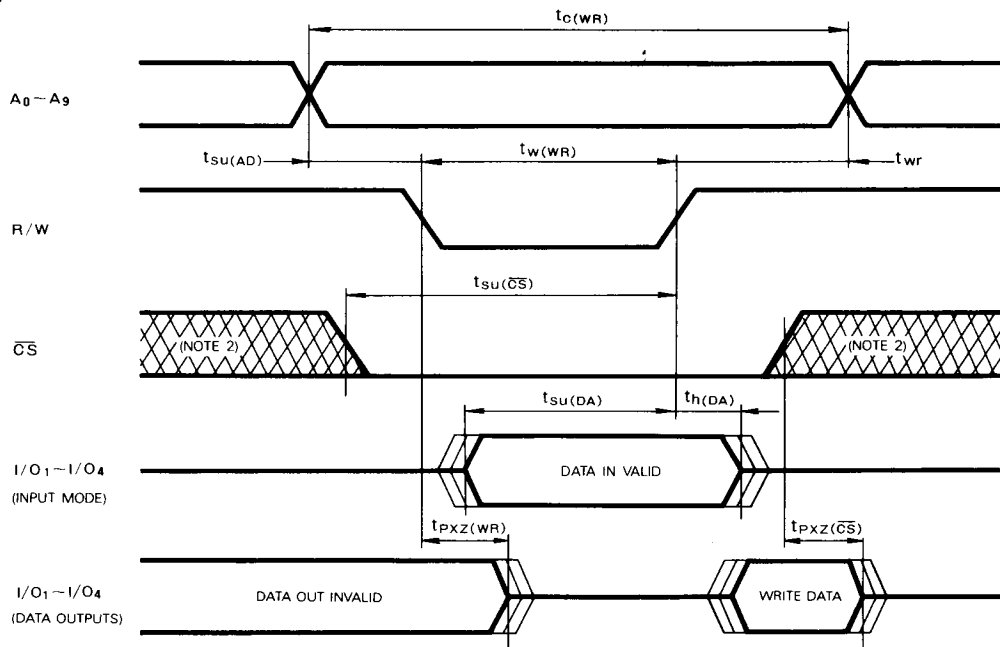
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TIMING DIAGRAMS

Read Cycle



Write Cycle



Note 2: Hatching indicates the state is unknown.



The center line indicates a floating (high-impedance) state.

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POWER-DOWN OPERATION

Electrical Characteristics (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VCC(PD)	Power-down supply voltage		2			V
VI(CS)	Power-down chip select input voltage	$2.2\text{ V} \leq V_{CC(PD)} \leq V_{CC}$	2.2			V
		$2\text{ V} \leq V_{CC(PD)} \leq 2.2\text{ V}$	VCC(PD)			V
ICC(PD)	Power-down supply current from VCC	VCC=2 V, all inputs = 2 V			15	μA

Note 3 : Current flowing into an IC is positive; out is negative.

Timing Requirements (Ta = 0 ~ 70°C, VCC=5V ± 10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
tsu(PD)	Power-down setup time	0			ns
tR(PD)	Power-down recovery time	tC(RD)			ns

Timing Diagram

