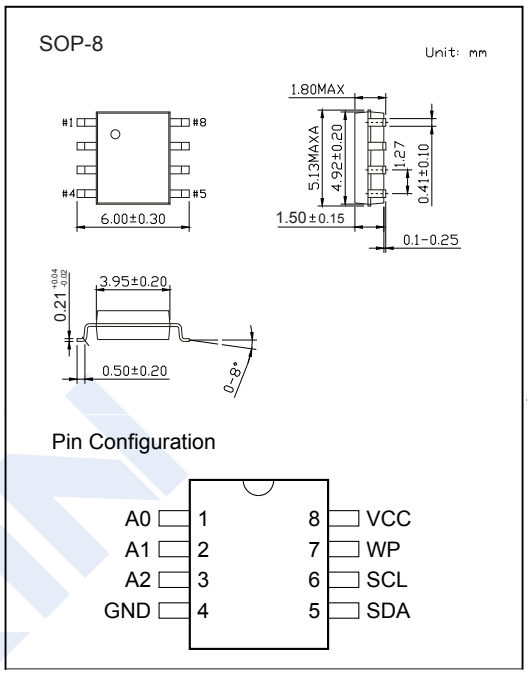
2KI²C™Serial EEPROM

AT24C02N

■ Features

- Single supply with operation down to 1.8v
- Low-power CMOS technology:
  - 1 mA active current, typical
  - 1 μA standby current, typical(I-temp)
- Organized as 1 block of 256 bytes (1×256×8)
- 2-wire serial interface bus, I²C™ compatible
- 400 kHz (24C02) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 8 bytes
- Can be operated as a serial ROM
- ESD protection>4,000V
- 1,000,000 erase/write cycles
- Data retention>200 years

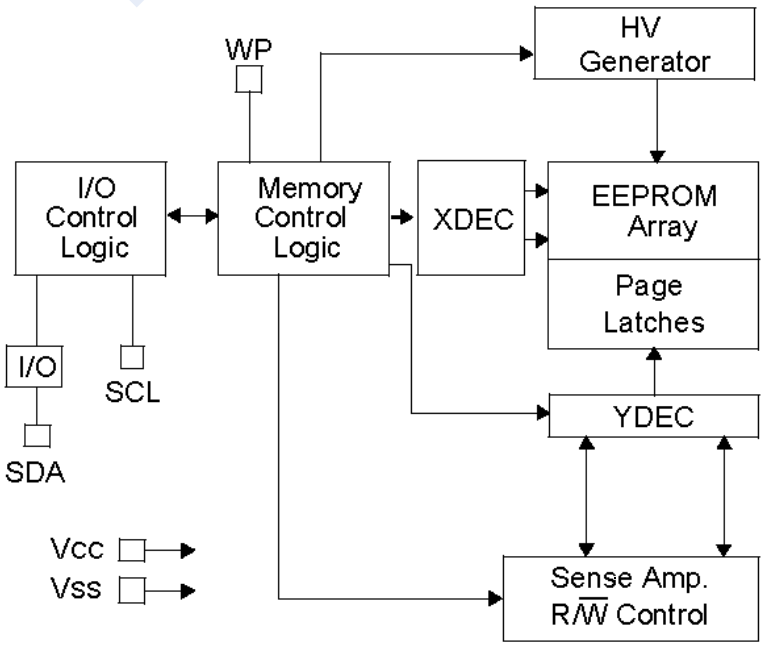


■ Device Selection Tble

Part Number	VCC Range	Max. Clock Frequency
AT24C02N	1.8-5.5	400 kHz

Note 1: 100 KHz for Vcc<1.8v

■ Block Diagram



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■ Absolute Maximum Ratings(t)

Vcc.....6.5v
All inputs and outputs w.r.t. Vss.....-0.3V to Vcc+1.0v
Storage temperature.....-50 ℃ to+125 ℃
Ambient temperature with power applied.....-25 ℃ to+75 ℃
ESD protection on all pins .....≥4KV

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

■ Table 1-1:DC Characteristis

DC Characteristis							
Param. NO.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
D1	VIH	**WP.SCL and SDA pins**					
D2		High-level input voltage	0.7 vcc			V	
D3	VIL	Low-level input voltage			0.3Vcc	V	
D4	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 Vcc			V	**(Note)**
D5	VOL	Low-level output voltage			0.40	V	IOL=3.0Ma,Vcc=1.8V
D6	ILI	Input leakage current			±1	uA	VIN=VSS or VCC
D7	ILO	Output leakage current			±1	uA	V_{OUT}=VSS or VCC
D8	CIN. COUT	Pin capacitance (all inputs/outputs)			10	pF	VCC=5.0V (**Note**) TA = 25℃,FCLK=1MHz
D9	Icc write	Operating current		0.1	3	mA	Vcc=5.5V,SCL=400kHz
D10	Icc read			0.05	1	mA	
D11	Iccs	Standby current		0.01	1	uA	Industrial
					5	uA	Automotive
							SDA=SCL=Vcc
							WP=Vss

Note: This parameter is periodically sampled and not 100% tested.

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■ Table 1-2:AC Characteristis

AC Characteristis							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency			400	kHz	1.8V≤ Vcc ≤ 5.5V
2	THIGH	Clock high time	600			ns	1.8V ≤ Vcc ≤ 5.5V
3	TLOW	Clock low time	1300			ns	1.8V ≤ Vcc ≤ 5.5V
4	TR	SDA and SCL rise time **(Note 1)**			300	ns	1.8V≤ Vcc ≤ 5.5V**(Note 1)**
5	TF	SDA and SCL fall time			300	ns	**(Note 1)**
6	THD:STA	Start condition hold time	600			ns	1.8V ≤ Vcc ≤ 5.5V
7	THD:STA	Start condition setup time	600			ns	1.8V ≤ Vcc ≤ 5.5V
8	THD:DAT	Data input hold time	0			ns	**(Note 2)**
9	TSU:DAT	Data input setup time	100			ns	1.8V ≤ Vcc ≤ 5.5V
10	TSU:STO	Stop condition setup time	600			ns	1.8V ≤ Vcc ≤ 5.5V
11	TAA	Output valid from clock **(Note2)**			900	ns	1.8V≤ Vcc ≤ 5.5V
12	TBUF	Bus free time:Time the Bus must be free before A new transmission can start	1300			ns	1.8V ≤ Vcc ≤ 5.5V
13	TOF	Output fall time from VIH Minimum to VIL maximum	20+0.1CB		250	ns	1.8V≤ Vcc ≤ 5.5V
14	TSP	Input filter spike Suppression (SDA and SCL pins)			50	ns	**(Notes 1 and 3)**
15	TWC	Write cycle time (byte or page)			5	ms	
16		Endurance	1M			cycles	25℃,**(Note 4)**

Note **1:** Not 100% tested. CB=total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintendcd gcncration of Start or Stop conditions.

3: The combined Tsp and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

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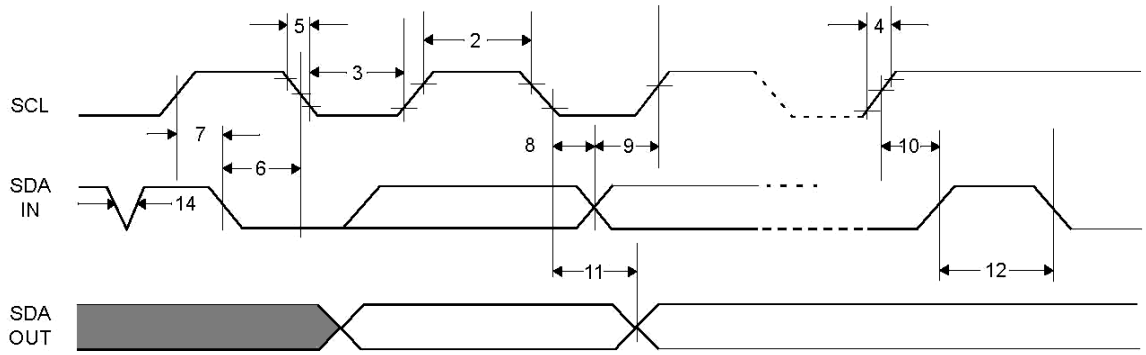
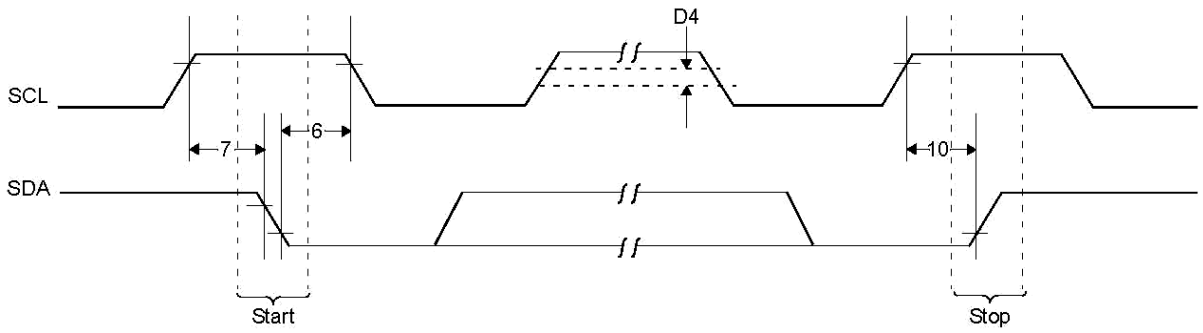
■ Typical Characterisitics

Figure 1-1:Bus Timing Data



a

Figure 1-2:Bus Timing Start/Stop



2.0 Functional Description

The 24C02 supports a bidirectional,2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the Serial Clock(SCL), controls the bus access and generates the Start and stop conditions, while the 24C02 wo rks as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 Bus Characteristics

The following bus protocol has been defined:

● Data transfer may be initiated only when the bus is not busy.

● During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined(Figure 3-1).

3.1 Bus Not Busy(A)

Both data and clock lines remain high.

3.2 Start Data Transfer(B)

A high-to-low transition of the SDA line while the clock(SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer(C)

A low-to-high transition of the SDA line while the clock(SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid(D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device and is, theoretically, unlimited (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur, it will replace data in a first-in first-out (FIFO) fashion.

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3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note: The 24C02 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledage clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24C02) will leave the data line high to enable the master to generate the Stop condition.

3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The control byte consists of a four-bit control code. For the 24C02, this is set as '1010' binary for read and write operations. The next three bites of the control byte are "don't cares" for the 24C02.

The last bit of the control byte defines the operation to be performed. When set to'1', a read operation is selected. When set to '0', a write operation is selected. Following the start condition, the 24C02 monito rs the SDA bus, checking the device type identifier being transmitted and ,upon a '1010' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C02 will select a read or write operation.

Operation	Control Code	Block Select	R/W
Read	1010	Block Address	1
Write	1010	Block Address	0

Figure 3-1:Data Transfer Sequence On The Serial Bus

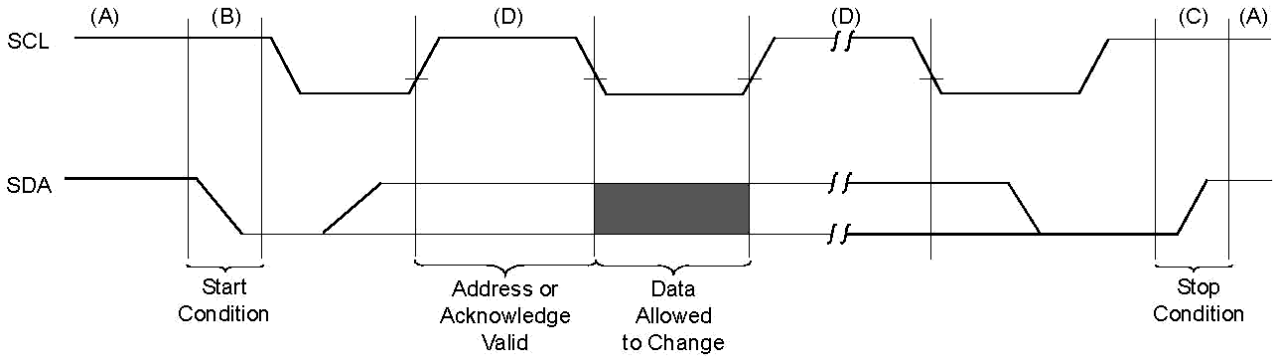
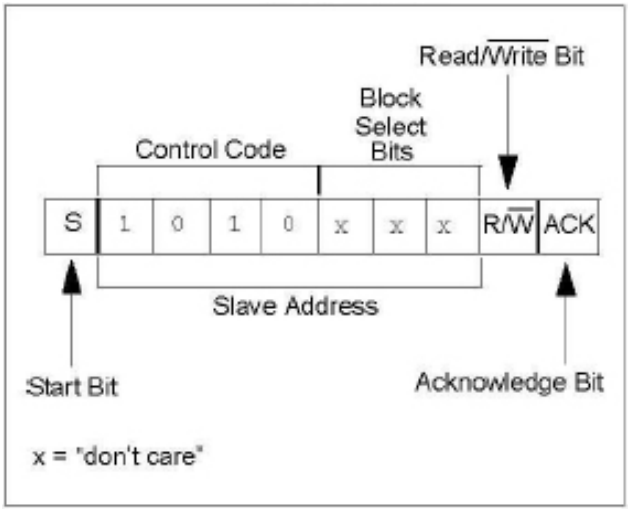


Figure 3-2:Control Byte Allocation



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4.0 Write Operation

4.1 Byte Write

Following the Start condition from the master , the device code (4 bits), the block address (3 bits, “don’t cares”) and the bit which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address Pointer of the 24C02. After receiving another Acknowledge signal from the 24C02, the master device will transmit the data word to be written into the addressed memory location. The 24C02 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle and, during this time, the 24C02 will not generate Acknowledge Signals (Figure 4-1).

4.2 Page Write

The write-control byte, word address and the first data byte are transmitted to the 24C02 in the same way as in a byte write. However, instead of generating a Stop condition, the master transmits up to 8 data bytes to the 24C02, which are temporarily stored in the on-chip page buffer and will be written into memory once the master has transmitted a Stop condition. Upon receipt of each word, the four lower-order Address Pointer bits are internally incremented by ‘1’. The higher-order 7 bits of the word address remain constant. If the master should transmit more than 8 words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 4-2).

Note: Page write operations are limited to writing bytes within a single physical page regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of [page size -1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

Figure 4-1:Byte Write

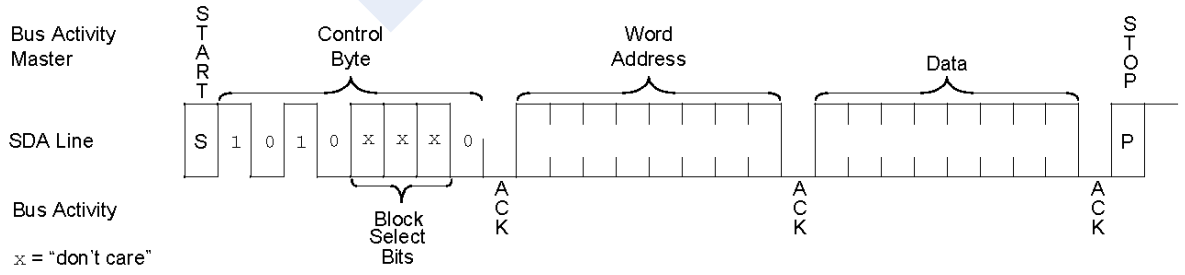
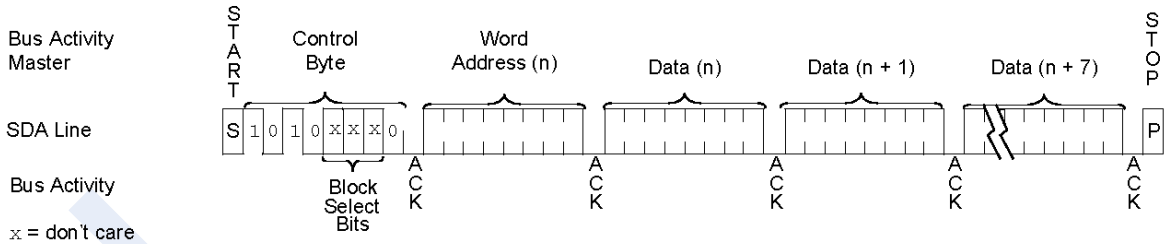


Figure 4-2:Page Write



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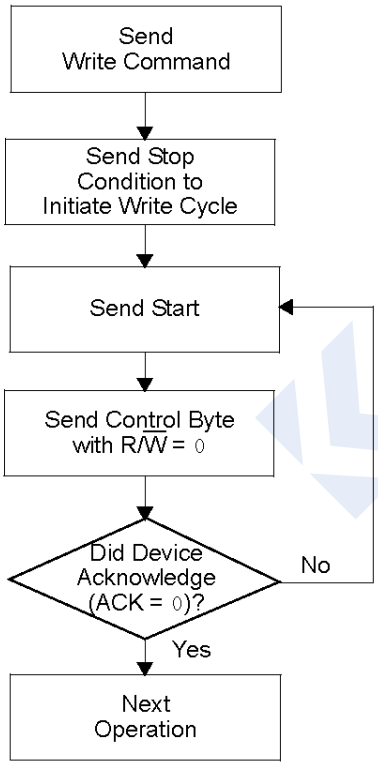
5.0 Acknowledge Polling

Since the device will not acknowledge during a write cycle ,this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally-timed write cycle and ACK polling can then be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command (=0). If the device is still busy with the write cycle, no ACK will be returned. If the cycle is complete, the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 5-1 for a flow diagram of this operation.

Figure 5-1: Acknowledge Polling Flow



6.0 Write Protection

The WP pin allows the user to write-protect the entire array (00-FF) when the pin is tied to Vcc. If tied to Vss, the write protection is disabled.

7.0 Read Operation

Read operations are initiated in the same way as write operations, with the exception that the bit of the slave address is set to '1'. There are three basic types of read operations; current address read, random read and sequential read.

7.1 Current Address Read

The 24C02 contains an address counter that maintains the address of the last word accessed. Internally incremented by '1'. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n+ 1, Upon receipt of the slave address bit set to '1', the 24C02 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition, and the 24C02 discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is accomplished by sending the word address to the 24C02 as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but bit set to a '1'. The 24C02 will then issue an acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition, and the 24C02 will discontinue transmission (figure 7-2).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read, except that once the 24C02 transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24C02 to transmit the next sequentially-addressed 8-bit word (Figure 7-3).
To provide sequential reads, the 24C02 contains an internal Address Pointer that is incremented by one upon completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24C02 employs a Vcc threshold detector circuit which disables the internal erase/write logic if the Vcc is below 1.5V at nominal conditions.
The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

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Figure 7-1:Current Address Read

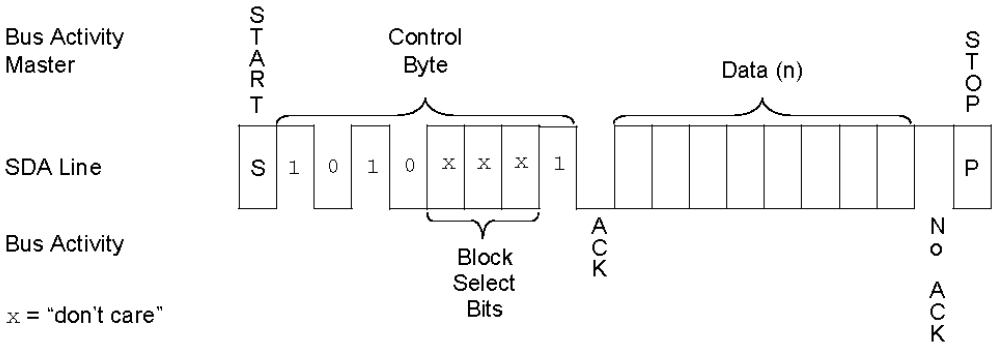


Figure 7-2:Random Read

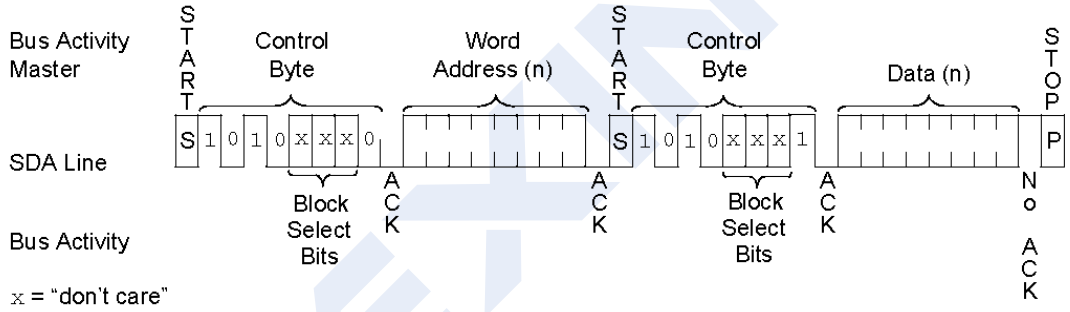
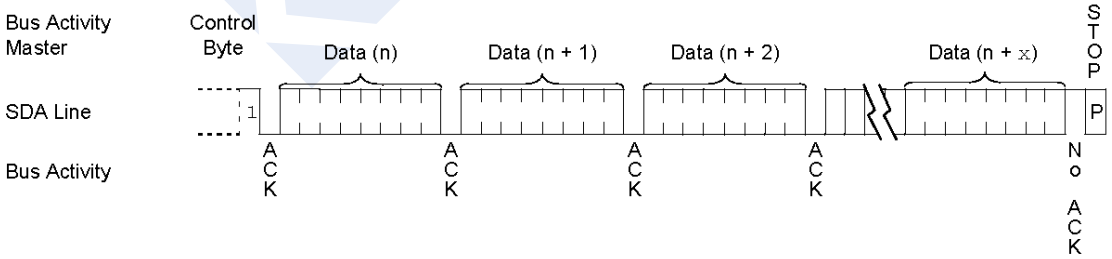


Figure 7-3:Sequential Read



8.0 Pin Descriptions

The descriptions of the pins are listed in Table 8-1.

Table 8-1: Pin Fubction Table

Name	Pin Number	Description
A0	1	Not Connected
A1	2	Not Connected
A2	3	Not Connected
Vss	4	Ground
SDA	5	Serial Address/Data I/O
SCL	6	Serial Clock
WP	7	Write-Protect Input
Vcc	8	+1.8V to 5.5V Power Supply

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8.1 Serial Address/Data Input/Output(SDA)
SDA is a bidirectional pin used to transfer addresses and data into and out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to Vcc (typical 10 KΩ for 100KHz, 2KΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low, Changes during SCL high are reserved for indicating Start and Stop conditions.

8.2 Serial Clock (SCL)
The SCL input is used to synchronize the data transfer to and from the device.

8.3 Write-Protect(WP)
The WP pin must be connected to either Vss or Vcc. If tied to Vss, normal memory operation is enabled (read/write the entire memory 00-FF).
If tied to Vcc, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

This feature allows the user to use the 24C02 as a serial ROM when WP is enabled (tied to Vcc).

8.4 A0,A1,A2
These A0,A1 and A2 pins are not used by the 24C02. They may be left floating or tied to either Vss or Vcc.