ICM7555

General purpose CMOS timer

Rev. 02 — 3 August 2009 Product data sheet

1. General description

The ICM7555 is a CMOS timer providing significantly improved performance over the standard NE/SE555 timer, while at the same time being a direct replacement for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$, and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL_VOLTAGE for stable operation.

The ICM7555 is a stable controller capable of producing accurate time delays or frequencies.

In the one-shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the NE/SE555 device, the CONTROL_VOLTAGE terminal need not be decoupled with a capacitor. The $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ inputs are active LOW. The output inverter can source or sink currents large enough to drive TTL loads or provide minimal offsets to drive CMOS loads.

2. Features

- Exact equivalent in most applications for NE/SE555
- Low supply current: 80 µA (typical)
- Extremely low trigger, threshold, and reset currents: 20 pA (typical)
- High-speed operation: 500 kHz guaranteed
- Wide operating supply voltage range guaranteed 3 V to 16 V over full automotive temperatures
- Normal reset function; no crowbarring of supply during output transition
- Can be used with higher-impedance timing elements than the NE/SE555 for longer time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Typical temperature stability of 0.005 % / °C at 25 °C
- Rail-to-rail outputs

3. Applications

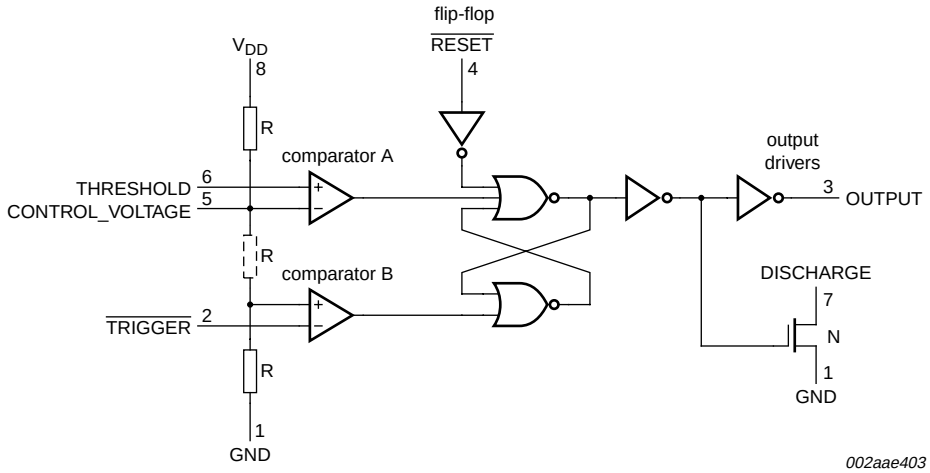
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

4. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
ICM7555CD	T_{amb} = 0 °C to +70 °C	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
ICM7555ID	T_{amb} = −40 °C to +85 °C			
ICM7555CN	T_{amb} = 0 °C to +70 °C	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
ICM7555IN	T_{amb} = −40 °C to +85 °C			

5. Functional diagram



Remark: Unused inputs should be connected to appropriate voltage from Table 3.

Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

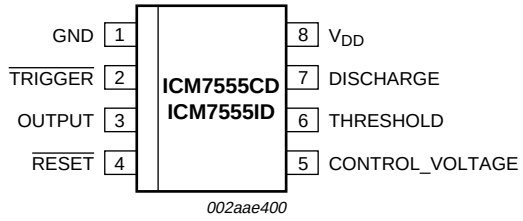


Fig 2. Pin configuration for SO8

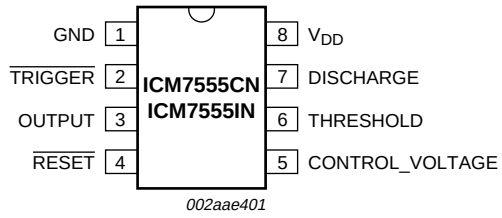


Fig 3. Pin configuration for DIP8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
GND	1	supply ground
$\overline{\text{TRIGGER}}$	2	start timer input; (active LOW)
OUTPUT	3	timer logic level output
$\overline{\text{RESET}}$	4	timer inhibit input; (active LOW)
CONTROL_VOLTAGE	5	timing capacitor upper voltage sense input
THRESHOLD	6	timing capacitor lower voltage sense input
DISCHARGE	7	timing capacitor discharge output
V_{DD}	8	supply voltage

7. Functional description

Refer to Figure 1 “Functional diagram”.

7.1 Function selection

Table 3. Function selection

THRESHOLD voltage	$\overline{\text{TRIGGER}}$ voltage	$\overline{\text{RESET}}$[1]	OUTPUT	Discharge switch
don’t care	don’t care	L	L	on
$> \frac{2}{3}$ V+	$> \frac{1}{3}$ V+	H	L	on
$V_{th} < \frac{2}{3}$ V+	$V_{trig} > \frac{1}{3}$ V+	H	stable	stable
don’t care	$< \frac{1}{3}$ V+	H	H	off

[1] $\overline{\text{RESET}}$ will dominate all other inputs; $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage				18	V
V_I	input voltage	$\overline{TRIGGER}$	[1]	–0.3	V_{DD} + 0.3	V
		CONTROL_VOLTAGE		–0.3	V_{DD} + 0.3	V
		THRESHOLD		–0.3	V_{DD} + 0.3	V
		$\overline{RESET}$		–0.3	V_{DD} + 0.3	V
I_O	output current			-	100	mA
P	power dissipation	T_{amb} = 25 °C (still air)	[2][3]			
		DIP8 package		-	1160	mW
		SO8 package		-	780	mW
T_{stg}	storage temperature			–65	+150	°C
T_{sp}	solder point temperature	soldering 60 s		-	300	°C

[1] Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} + 0.3 V or less than GND – 0.3 V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555 must be turned on first.

[2] Above 25 °C, derate at the following rates:
DIP8 package at 9.3 mW / °C
SO8 package at 6.2 mW / °C

[3] Refer to Section 11.2 “Power supply considerations” section.

9. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	$T_{min} \le T_{amb} \le T_{max}$	3	-	16	V
I_{DD}	supply current[1]	$V_{DD} = V_{min}$	-	50	200	µA
		$V_{DD} = V_{max}$	-	180	300	µA
Astable mode timing[2][3]						
Δf/f	frequency stability		-	1.0	5.0	%
Δf/ΔV	frequency variation with voltage		-	0.1	3.0	%/V
Δf/ΔT	frequency variation with temperature[4]	V_{DD} = 5 V	-	50	-	ppm/°C
		V_{DD} = 10 V	-	75	-	ppm/°C
		V_{DD} = 15 V	-	100	-	ppm/°C
V_I	input voltage	$\overline{TRIGGER}$: V_{DD} = 5 V	0.29V_{DD}	0.31V_{DD}	0.34V_{DD}	V
		CONTROL_VOLTAGE: V_{DD} = 5 V	0.62V_{DD}	0.65V_{DD}	0.67V_{DD}	V
		THRESHOLD: V_{DD} = 5 V	0.63V_{DD}	0.65V_{DD}	0.67V_{DD}	V
		$\overline{RESET}$: $V_{DD} = V_{min}$ and V_{max}	0.4V_{DD}	0.7V_{DD}	1.0V_{DD}	V

Table 5. Characteristics *...continued*

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input current	$\overline{\text{TRIGGER}}$				
		$V_{DD} = V_{trig} = V_{max}$	-	50	-	pA
		$V_{DD} = V_{trig}$ = 5 V	-	10	-	pA
		$V_{DD} = V_{trig} = V_{min}$	-	1	-	pA
		THRESHOLD				
		$V_{DD} = V_{th} = V_{max}$	-	50	-	pA
		$V_{DD} = V_{th}$ = 5 V	-	10	-	pA
		$V_{DD} = V_{th} = V_{min}$	-	1	-	pA
		$\overline{\text{RESET}}$				
		$V_{DD} = V_{rst} = V_{max}$	-	100	-	pA
		$V_{DD} = V_{rst}$ = 5 V	-	20	-	pA
		$V_{DD} = V_{rst} = V_{min}$	-	2	-	pA
V_{OL}	LOW-level output voltage	$V_{DD} = V_{max}$; I_{sink} = 3.2 mA	-	0.1	0.4	V
		V_{DD} = 5 V; I_{sink} = 3.2 mA	-	0.2	0.4	V
V_{OH}	HIGH-level output voltage	I_{source} = −1.0 mA				
		$V_{DD} = V_{max}$	15.25	15.7	-	V
		V_{DD} = 5 V_{max}	4.0	4.5	-	V
V_o	output voltage	DISCHARGE: V_{DD} = 5 V; I_{DIS} = 10 mA	-	0.2	0.4	V
$t_{r(o)}$	output rise time[4]	R_L = 10 MΩ; C_L = 10 pF; V_{DD} = 5 V	-	45	75	ns
$t_{f(o)}$	output fall time[4]		-	20	75	ns
f_{osc}	oscillator frequency	astable mode	-	-	500	kHz

[1] The supply current value is essentially independent of the $\overline{\text{TRIGGER}}$, THRESHOLD and $\overline{\text{RESET}}$ voltages.

[2] Astable timing is calculated using the following equation:

$$f = \frac{1.38}{(R_A + 2R_B)C}$$

The components are defined in Figure 15.

[3] R_A, R_B = 1 kΩ to 100 kΩ; C = 0.1 µF; 5 V < V_{DD} < 15 V

[4] Parameter is not 100 % tested.

10. Typical performance curves

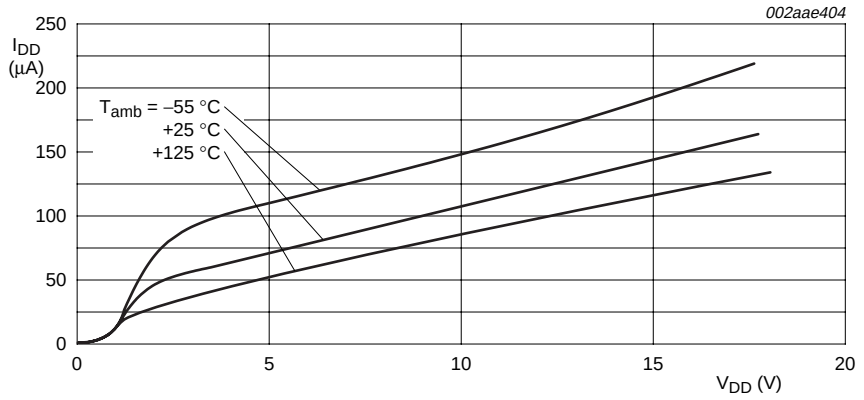
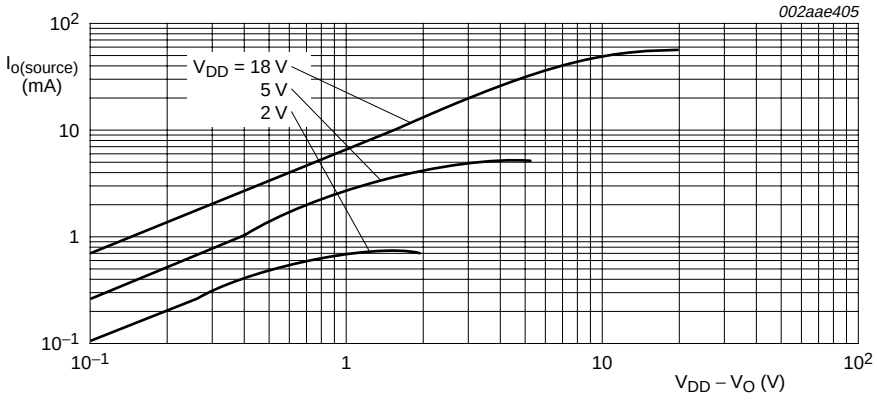
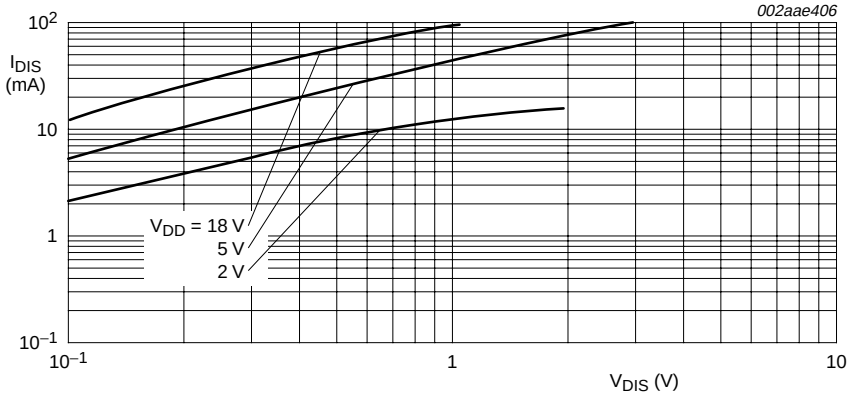


Fig 4. Supply current versus supply voltage



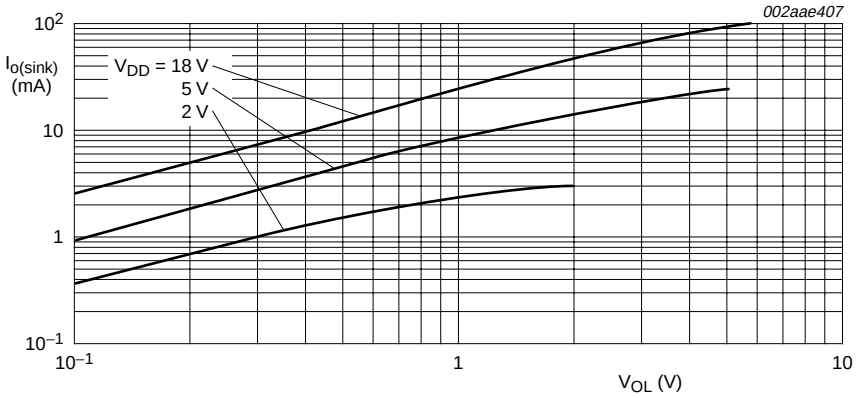
T_{amb} = +25 °C.

Fig 5. High output voltage drop versus output source current

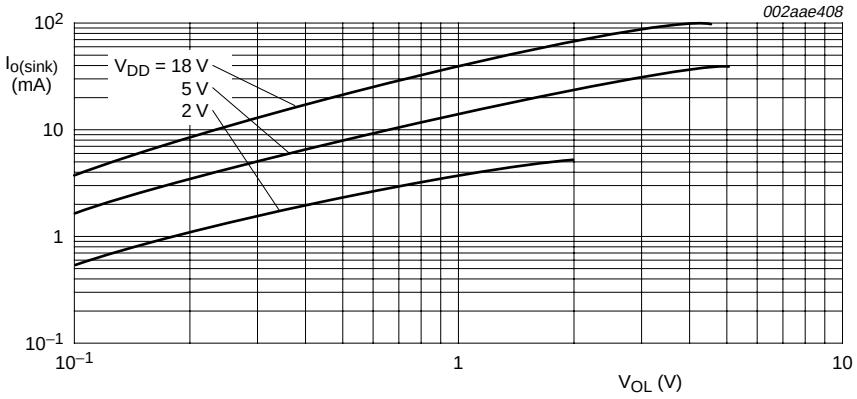


T_{amb} = +25 °C.

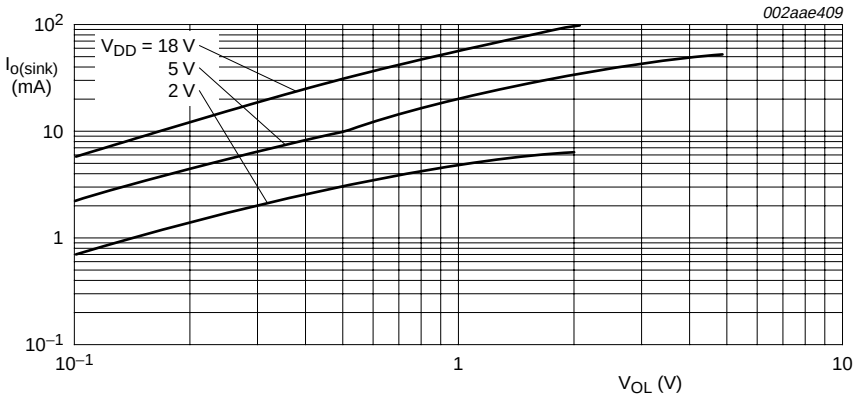
Fig 6. Discharge low output voltage versus discharge sink current



a. T_{amb} = +125 °C.



b. T_{amb} = +25 °C.



c. T_{amb} = –55 °C.

Fig 7. Low output voltage versus output sink current

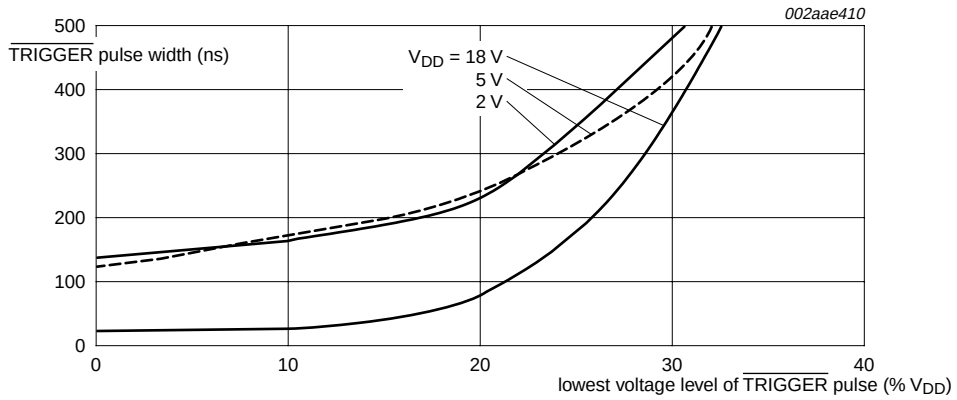


Fig 8. Minimum pulse width for triggering

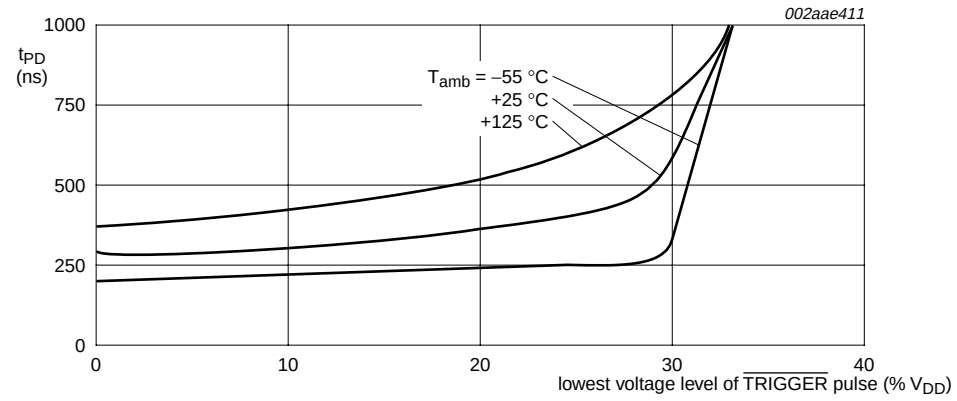
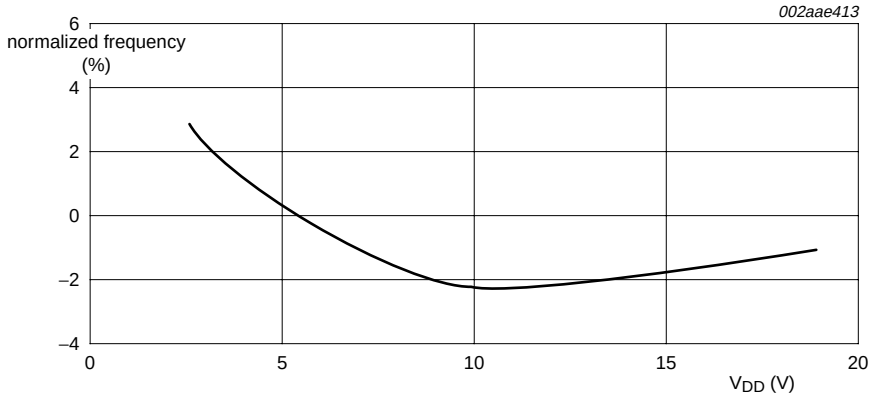


Fig 9. Propagation delay versus voltage level of $\overline{\text{TRIGGER}}$ pulse (V_{DD} = 5 V)

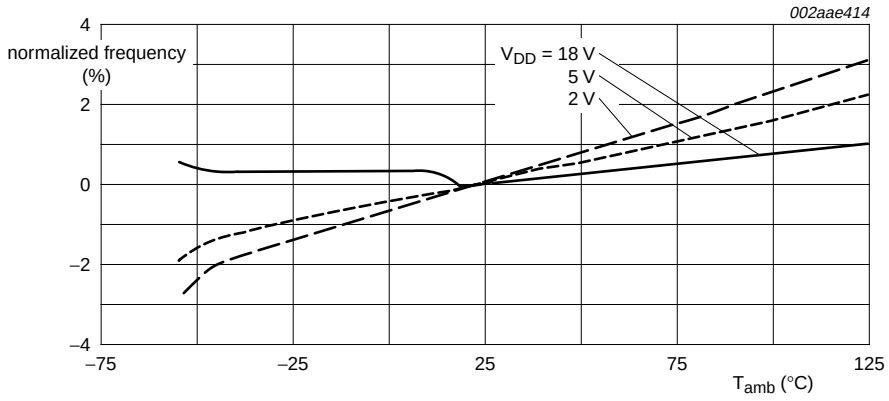


T_{amb} = +25 °C

$R_A = R_B$ = 10 kΩ

C = 0.1 µF

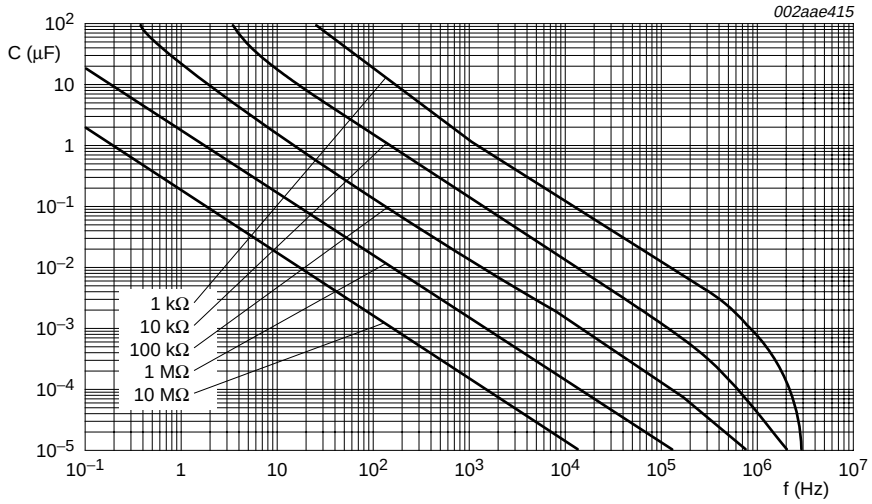
Fig 10. Normalized frequency stability as a function of supply voltage (astable mode)



$R_A = R_B$ = 1 kΩ

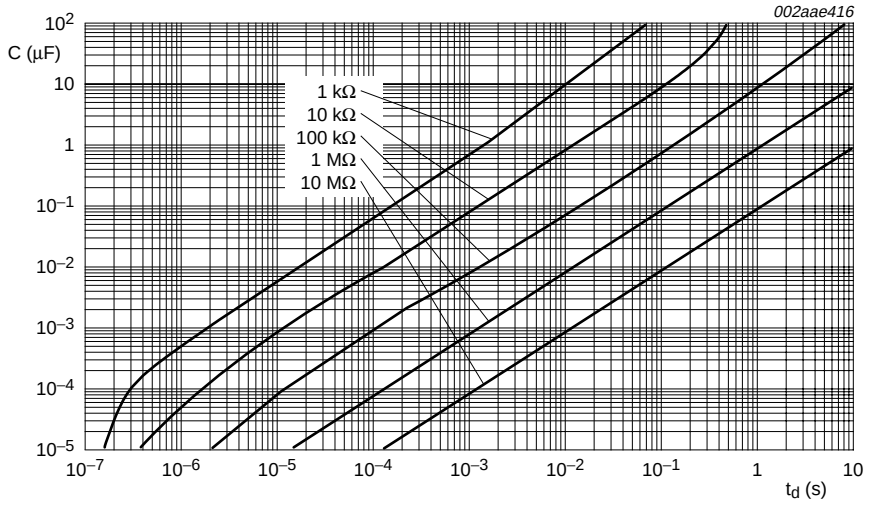
C = 0.1 µF

Fig 11. Normalized frequency stability as a function of temperature (astable mode)



V_{DD} = 5 V; T_{amb} = +25 °C

Fig 12. Free-running frequency as a function of R_A, R_B resistance and external capacitance



V_{DD} = 5 V; T_{amb} = +25 °C

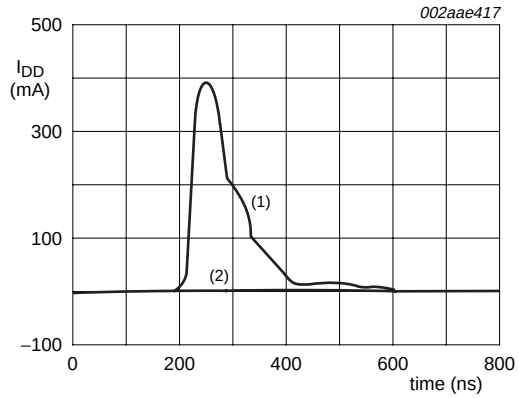
Fig 13. Monostable time delay versus R_A resistance and external capacitance

11. Application information

11.1 General

The ICM7555 device is, in most instances, a direct replacement for the NE/SE555 device. However, it is possible to effect economies in the external component count using the ICM7555. Because the NE/SE555 device produces large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The ICM7555 device produces no such transients. See Figure 14.

The ICM7555 produces supply current spikes of only 2 mA to 3 mA instead of 300 mA to 400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL_VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, 2 capacitors can be saved using an ICM7555.



T_{amb} = +25 °C

(1) NE/SE555

(2) ICM7555

Fig 14. Supply current transient compared with a standard NE/SE555 device during an output transition

11.2 Power supply considerations

Although the supply current consumed by the ICM7555 device is very low, the total system supply can be high unless the timing components are high-impedance. Therefore, high values for R and low values for C in Figure 15 and Figure 16 are recommended.

11.3 Output drive capability

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 V or more, the ICM7555 will drive at least 2 standard TTL loads.

11.4 Astable operation

If the circuit is connected as shown in Figure 15, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus, the duty cycle (δ) may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between $^1/_3$ V_{DD} and $^2/_3$ V_{DD}. Since the charge rate and the threshold levels are directly proportional to the supply voltage, the frequency of oscillation is independent of the supply voltage.

$$f = \frac{1.38}{(R_A + 2R_B) \times C} \quad (1)$$

$$\delta = \frac{R_A + R_B}{R_A + 2R_B} \quad (2)$$

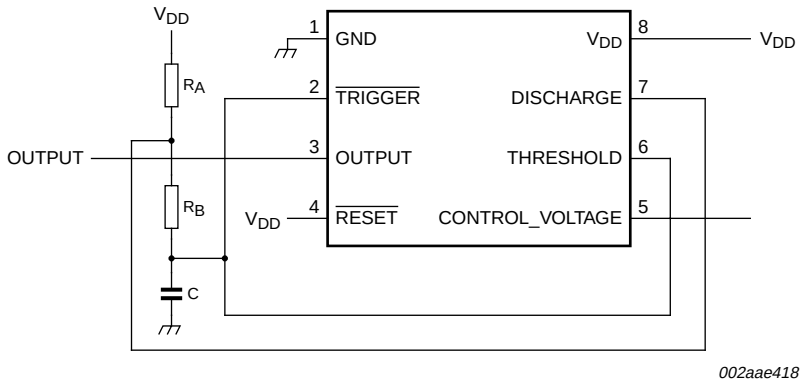
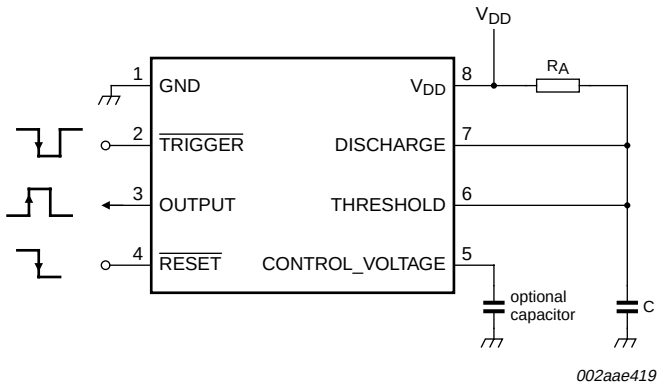


Fig 15. Astable operation

11.5 Monostable operation

In this mode of operation, the timer functions as a one-shot. Initially, the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative pulse to pin 2, $\overline{\text{TRIGGER}}$, the internal flip-flop is set, which releases the low-impedance on DISCHARGE; the external capacitor charges and drives the OUTPUT HIGH. The voltage across the capacitor increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its LOW state. $\overline{\text{TRIGGER}}$ must return to a HIGH state before the OUTPUT can return to a LOW state.



$V_{DD} \leq 18$ V; $t = 1.05\ R_A C$

Fig 16. Monostable operation

11.6 Control voltage

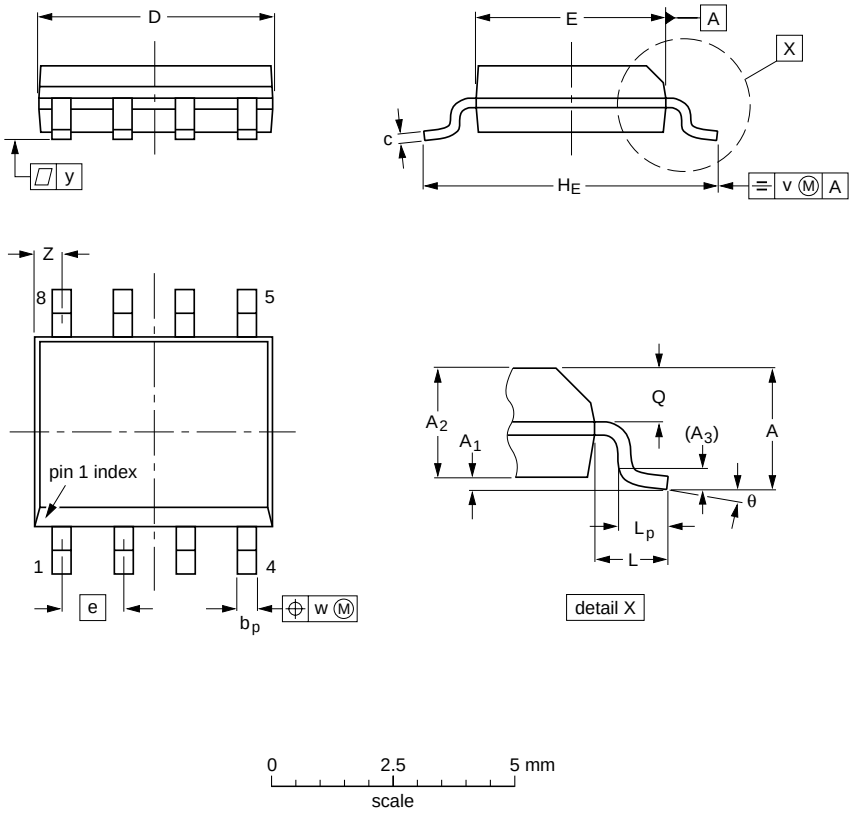
The CONTROL_VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode, or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL_VOLTAGE pin.

11.7 $\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard NE/SE555 device, i.e., 0.6 V to 0.7 V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard NE/SE555 device in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the NE/SE555 devices.

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

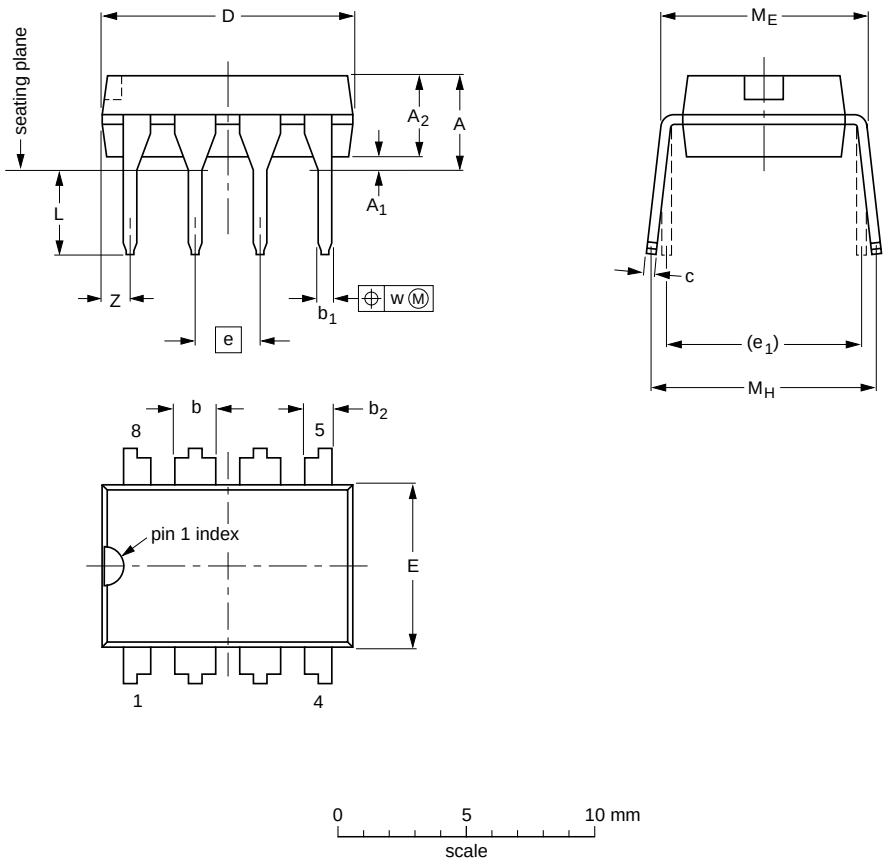
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 17. Package outline SOT96-1 (SO8)

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13

Fig 18. Package outline SOT97-1 (DIP8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6 and 7

Table 6. SnPb eutectic process (from J-STD-020C)

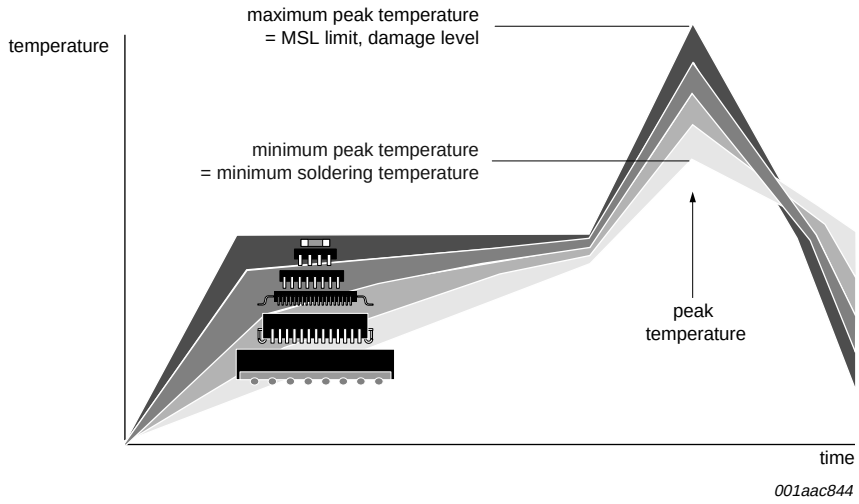
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Soldering of through-hole mount packages

14.1 Introduction to soldering through-hole mount packages

This text gives a very brief insight into wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 8. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductors
TTL	Transistor-Transistor Logic
SCR	Silicon-Controlled Rectifier

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ICM7555_2	20090803	Product data sheet	-	ICM7555_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Provided separate pinning diagrams for SO8 and DIP8 packages (Figure 2 and Figure 3, respectively). • Added Table 2 “Pin description”. • Table 4 “Limiting values”: – Symbols V_{TRIG}, V_{CV}, V_{TH}, V_{RST} are replaced with V_I (specific pin names are now noted under Conditions column). – Symbol/parameter “P_{DMAX}, maximum power dissipation” replaced with “P, power dissipation” (only maximum values given). – Symbol/parameter “T_{STG}, storage temperature range” replaced with “T_{stg}, storage temperature”. – Symbol changed from “T_{SOLD}” to “T_{sp}, solder point temperature” • Table 5 “Characteristics”: – Symbols Δf/f, Δf/ΔV, Δf/ΔT, have been added for Astable mode timing. – Symbols V_{TRIG}, V_{CV}, V_{TH}, V_{RST} are replaced with V_I (specific pin names are now noted under Conditions column). – Symbols I_{TRIG}, I_{TH}, I_{RST} are replaced with I_I (specific pin names are now noted under Conditions column). – Symbol/parameter “V_{DIS}, discharge output voltage” changed to “V_o, output voltage” (specific pin name is now noted under Conditions column). – Symbol/parameter “t_R, rise time of output” changed to “$t_{r(o)}$, output rise time”. – Symbol/parameter “t_F, fall time of output” changed to “$t_{f(o)}$, output fall time”. – Symbol “F_{MAX}” changed to “f_{osc}, oscillator frequency”. • Section 11.4 “Astable operation”: changed symbol for duty cycle from “D” to “δ”. • Added Section 12 “Package outline”. • Added soldering information. • Added Section 15 “Abbreviations”.			
ICM7555_1	19940831	Product specification	ECN 853-1192 13721 dated 1994 Aug 31	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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