

## MOS FIELD EFFECT TRANSISTOR 2SK2485

#### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **DESCRIPTION**

The 2SK2485 is N-Channel MOS Field Effect Transistor designed www.DataSheet4U.confor high voltage switching applications.

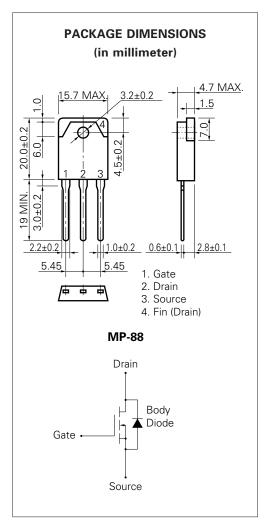
#### **FEATURES**

- Low On-Resistance RDS (on) = 2.8  $\Omega$  (VGS = 10 V, ID = 3.0 A)
- Low Ciss Ciss = 1 200 pF TYP.
- High Avalanche Capability Ratings

#### ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	$V_{\text{DSS}}$	900	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	ID (DC)	$\pm 6.0$	Α
Drain Current (pulse)*	ID (puls	e) ±12	Α
Total Power Dissipation (Tc = 25 °C)	P <sub>T1</sub>	100	W
Total Power Dissipation (T <sub>A</sub> = 25 °C)	P <sub>T2</sub>	3.0	W
Channel Temperature	$T_ch$	150	°C
Storage Temperature	$T_{stg}$	–55 to +150	°C
Single Avalanche Current**	las	6.0	Α
Single Avalanche Energy**	Eas	42.3	mJ

- \* PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
- \*\* Starting T<sub>ch</sub> = 25 °C, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20 V  $\rightarrow$  0



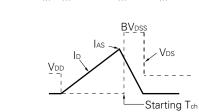


#### ELECTRICAL CHARACTERISTICS (TA = 25 °C)

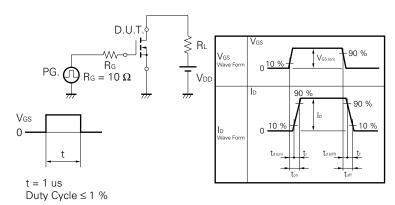
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS (on)		2.2	2.8	Ω	Vgs = 10 V, ID = 3.0 A
Gate to Source Cutoff Voltage	VGS (off)	2.5		3.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	2.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.0 A
Drain Leakage Current	Ipss			100	μΑ	V <sub>DS</sub> = V <sub>DSS</sub> , V <sub>GS</sub> = 0
Gate to Source Leakage Current	Igss			±100	nA	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
Input Capacitance	Ciss		1200		pF	V <sub>DS</sub> = 10 V
Output Capacitance	Coss		170		pF	V <sub>G</sub> S = 0
Reverse Transfer Capacitance	Crss		30		pF	f = 1 MHz
4Turn-On Delay Time	td (on)		20		ns	ID = 3.0 A
Rise Time	tr		10		ns	V <sub>G</sub> S = 10 V
Turn-Off Delay Time	td (off)		70		ns	V <sub>DD</sub> = 150 V
Fall Time	tf		15		ns	$R_G = 10 \Omega R_L = 50 \Omega$
Total Gate Charge	Q <sub>G</sub>		40		nC	ID = 6.0 A
Gate to Source Charge	Qgs		7		nC	V <sub>DD</sub> = 450 V
Gate to Drain Charge	Q <sub>GD</sub>		17		nC	V <sub>G</sub> S = 10 V
Body Diode Forward Voltage	VF (S-D)		1.0		V	IF = 6.0 A, VGS = 0
Reverse Recovery Time	trr		740		ns	IF = 6.0 A, VGS = 0
Reverse Recovery Charge	Qrr		4.0		μC	di/dt = 50 A/μs

#### **Test Circuit 1 Avalanche Capability**

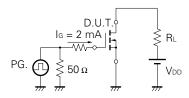
# $V_{GS} = 20 - 0 \text{ V}_{M}$ $V_{GS} = 20 - 0 \text{ V}_{M}$ $V_{DS} = 20 - 0 \text{ V}_{M}$ $V_{DS} = 20 - 0 \text{ V}_{M}$



#### **Test Circuit 2 Switching Time**

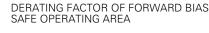


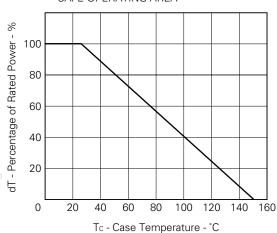
#### **Test Circuit 3 Gate Charge**



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

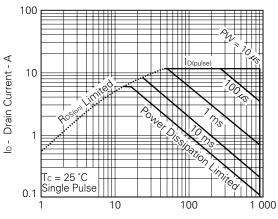
#### TYPICAL CHARACTERISTICS (TA = 25 °C)





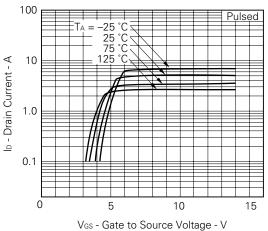
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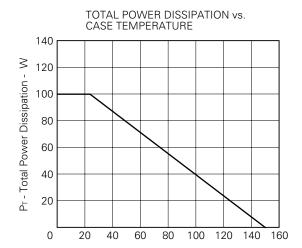
#### FORWARD BIAS SAFE OPERATING AREA



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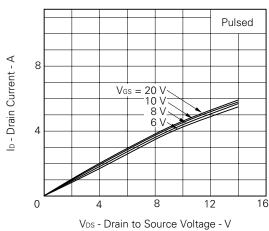
#### FORWARD TRANSFER CHARACTERISTICS





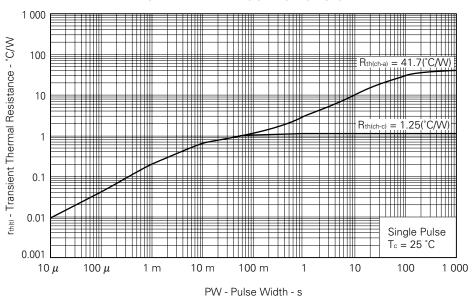
#### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

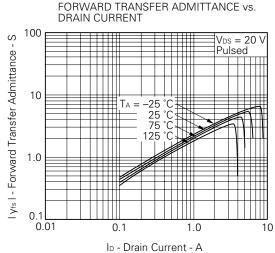
Tc - Case Temperature - °C

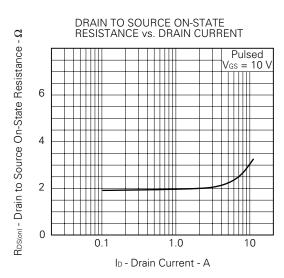




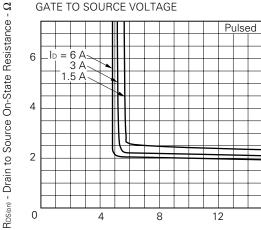
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





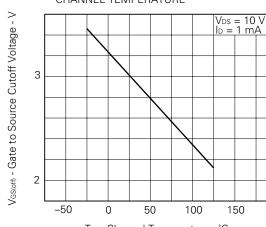


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

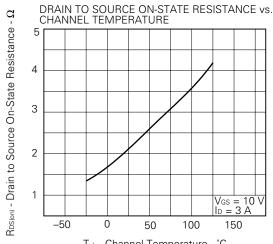


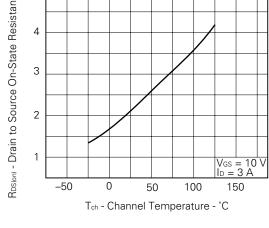
V<sub>GS</sub> - Gate to Source Voltage - V

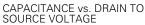
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

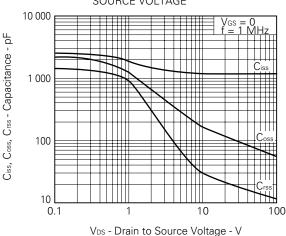


 $T_{\text{ch}}$  - Channel Temperature -  $^{\circ}\text{C}$ 

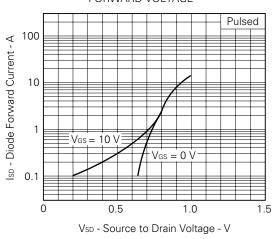




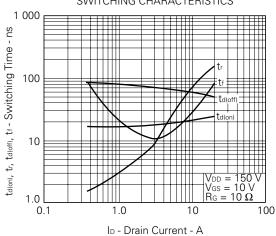




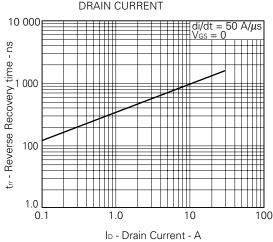
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



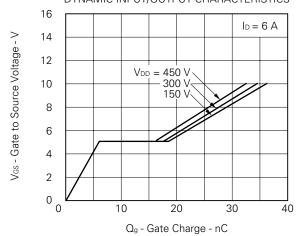
SWITCHING CHARACTERISTICS

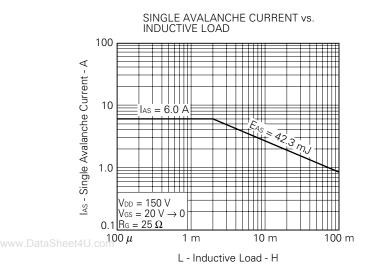


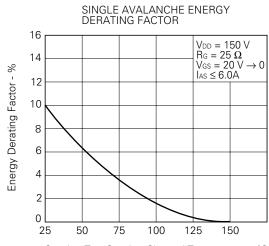
### REVERSE RECOVERY TIME vs. DRAIN CURRENT



#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS







Starting T  $_{\text{ch}}$  - Starting Channel Temperature -  $^{\circ}\text{C}$ 



#### REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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Anti-radioactive design is not implemented in this product.

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