NEC
ELECTRON DEVICE

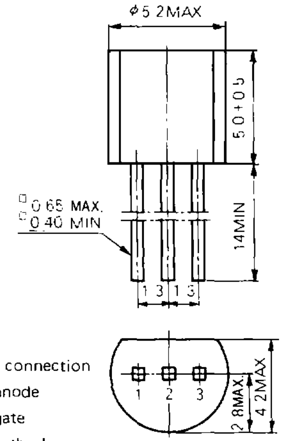
PUT
N13T1, N13T2

PROGRAMMABLE UNIJUNCTION TRANSISTOR
Silicon Planar Type N-gate Thyristor

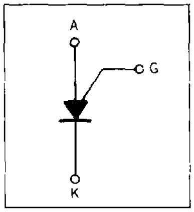
The N13T1, T2 are planar type PUT for the industrial use. The designer can select the resistance values to program the characteristics such as R_{BB}, η, I_V, and I_P to meet his particular needs.

Application of the N13T includes thyristor trigger, timing circuits, oscillator, pulse generator, sensing circuit and other N-gate thyristors.

Outline Drawing (Unit : mm)



lead connection
1. anode
2. gate
3. cathode



FEATURES

- N gate SCR which has high gate sensitivity.
- Low leakage current.
- Wide changeability R_{BB}, η, I_P, I_V.
- Low in I_V and small power operation.
- Fast, High Energy Trigger Pulse.
- Low cost.

MAXIMUM ALLOWABLE RATINGS (Ta = 25°C)

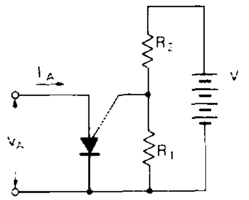
Items	Symbols	Specifications	Unit
Gate-Cathode Forward Voltage	V_{GKF}	40	V
Gate-Cathode Reverse Voltage	V_{GKR}	5	V
Gate-Anode Reverse Voltage	V_{GAR}	40	V
Anode-Cathode Voltage	V_{AK}	±40	V
DC Anode Current *1	I_T	150	mA
DC Gate Current *1	I_G	±20	mA
Peak Anode Recurrent *2 Pulse width 100μs, duty 1% Pulse width 20μs, duty 1%	I_{TRM}	1.0 2.0	A A
Peak Anode Non-recurrent Pulse width 10μs	I_{TSM}	5.0	A
Total Average Power *1	P_T	300	mW
Operation Ambient Temperature Range	T_{opt}	−50 ~ +100	°C
Junction Temperature	T_j	125	°C
Capacitive Discharge Power *3	E	250	μJ

Note: Please refer to Application Note No. 3; PUT application.
*1 Derate currents and powers 1%/°C above 25°C
*2 Rectangular wave.
*3 $E = 1/2\ CV^2$ capacitor discharge energy no current limiting.

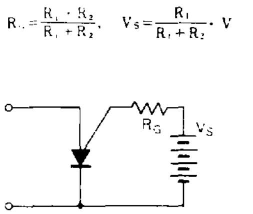
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Items		Symbol	Fig. No.	Type No.	MIN.	TYP.	MAX.	Unit
Peak Current (V_S = 10V)	R_G = 1MΩ	I_P	Fig.1, Fig.2, Fig.3, Fig.6, Fig.9	N12T1			2	μA
				N13T2			0.15	
	R_G = 10KΩ			N13T1			5	
				N13T2			1.0	
Offset Voltage (V_S = 10V)	R_G = 1MΩ	V_T	Fig.1	N13T1	0.2		1.6	V
				N13T2	0.2		0.6	
	R_G = 10KΩ		Fig.10	N13T1	0.2		0.6	
				N13T2	0.2		0.6	
Valley Current (V_S = 10V)	R_G = 1MΩ	I_V	Fig.1, Fig.4, Fig.5, Fig.7, Fig.8	N13T1			50	μA
				N13T2			25	
	R_G = 10KΩ			N13T1	70			
				N13T2	25			
Gate-Anode Leakage Current (K Open, V_S = 40V)		I_{GAO}	Fig.12			0.03	10	nA
Gate-Cathode Leakage Current (A–K Short, V_S = 40V)		I_{GKS}	Fig.12			0.3	100	nA
Forward Voltage (I_F = 50mA)		V_F	Fig.1, Fig.17			1	1.5	V
Pulse Out-put Voltage (V = 20V, C = 0.2μF)		V_O	Fig.14, Fig.15		6	10		V
Pulse Voltage Rate of Rise (V = 20V, C = 0.2μF)		t_r	Fig.1			50	80	ns

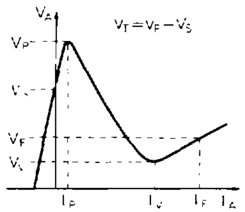
Fig. 1 Definition of Electrical Characteristic



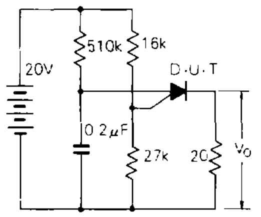
(1a) Equivalent UJT which is connected Program resistance.



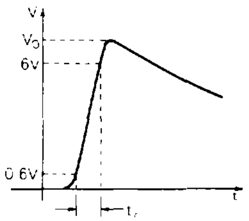
(1b) The definition of equivalent circuit of (1a) and VS, RG.



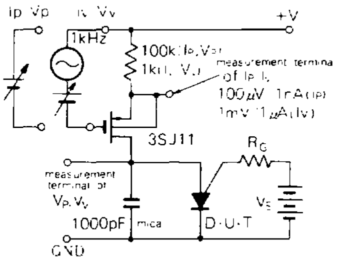
(1c) Characteristic model of VA–IA and the definition of measurement point.



(1d) Vo, tr measurement circuit.



(1e) The definition of output pulse wave and measurement point.



(1f) Measurement method of IP, VP, IV, VV
(Please refer to Application Note No 3)

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Fig. 2 N13T1 IP–RG Typical Characteristic (VS=10V)

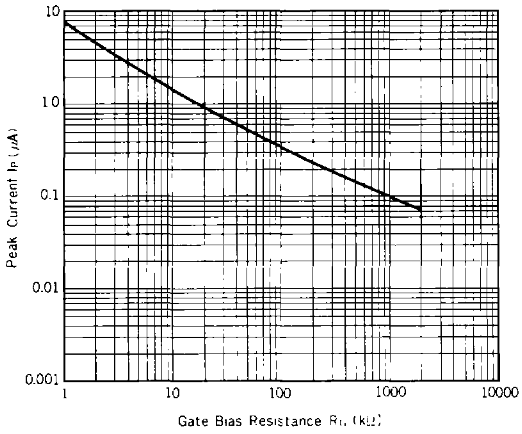

Fig. 3 N13T2 IP–RG Typical Characteristic (VS=10V)

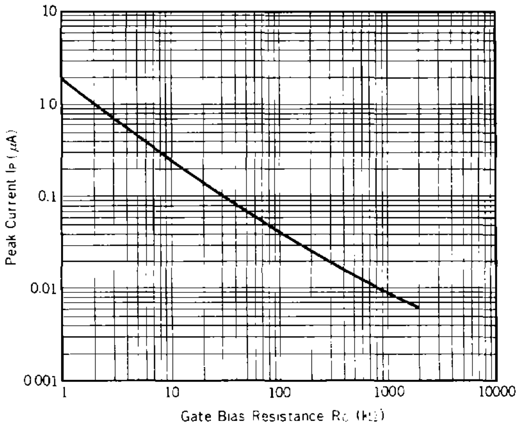

Fig. 4 N13T1 Iv–RG Typical Characteristic

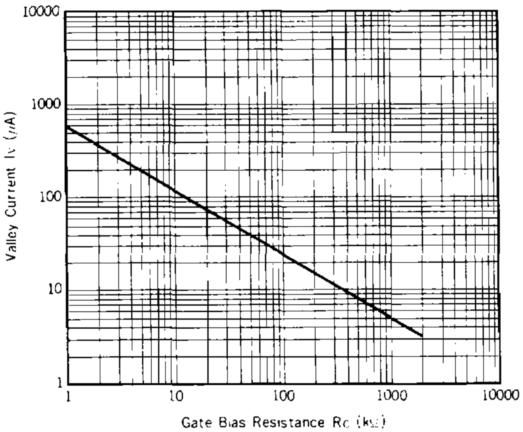

Fig. 5 Iv –RG Typical Characteristic

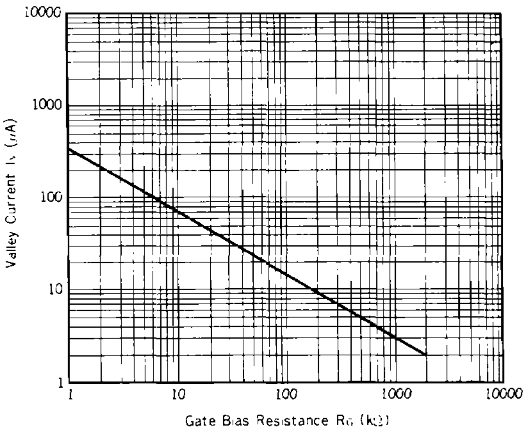

Fig. 6 IP–Ta–RG Typical Characteristic (VS=10V)

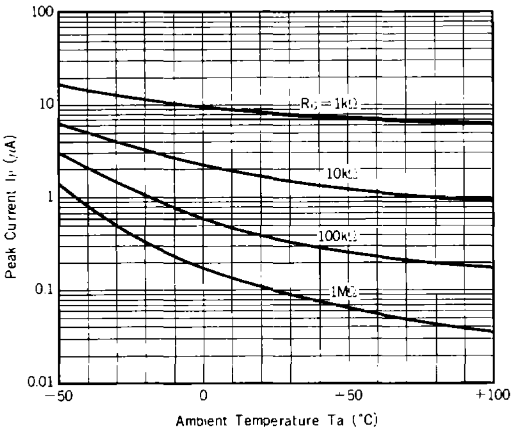

Fig. 7 Iv –Ta–RG Typical Characteristic (VS=10V)

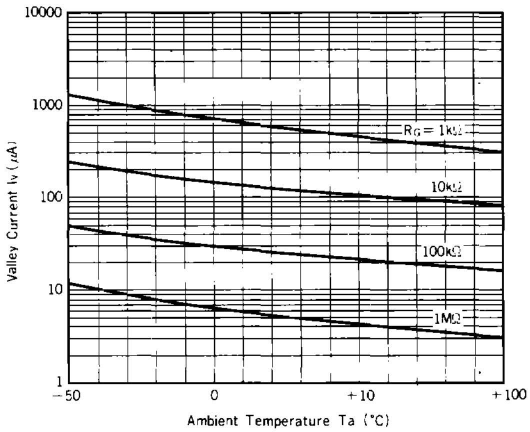

Fig. 8 I_V–V_S–R_G Typical Characteristic

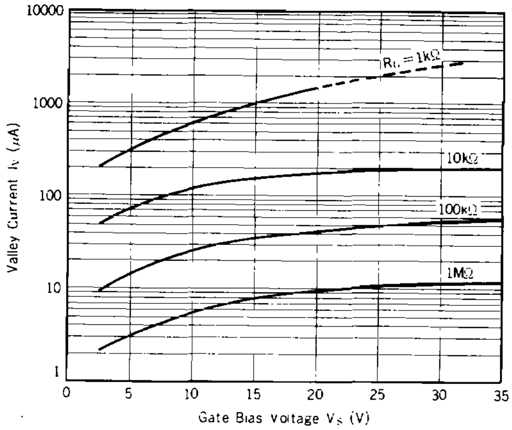

Fig. 9 I_P–V_S–R_G Typical Characteristic

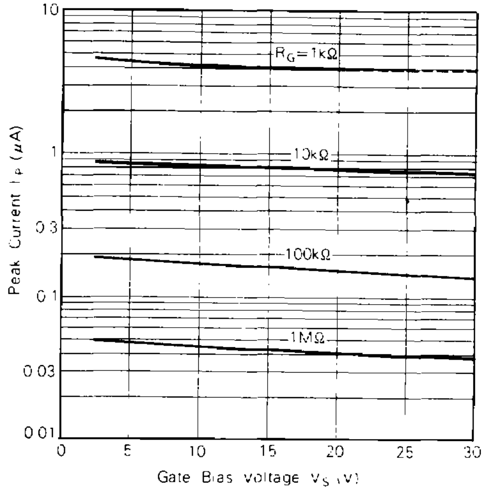

Fig. 10 V_T–R_G–Ta Typical Characteristic (V_S=10V)

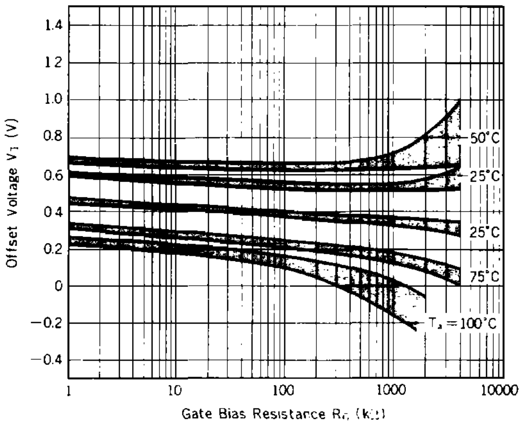

Fig. 11 V_V–Ta–R_G Typical Characteristic (V_S=10V)

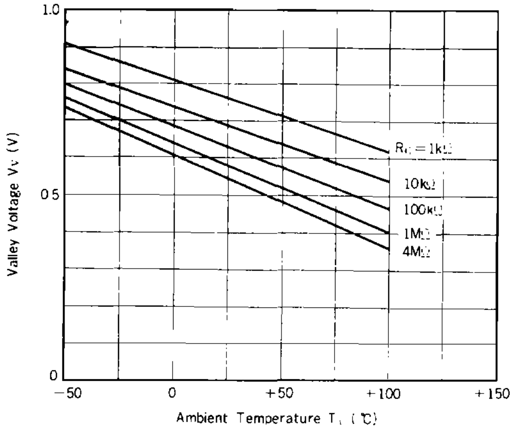

Fig. 12 I_{leak}–Ta Typical Characteristic (V_S=40V)

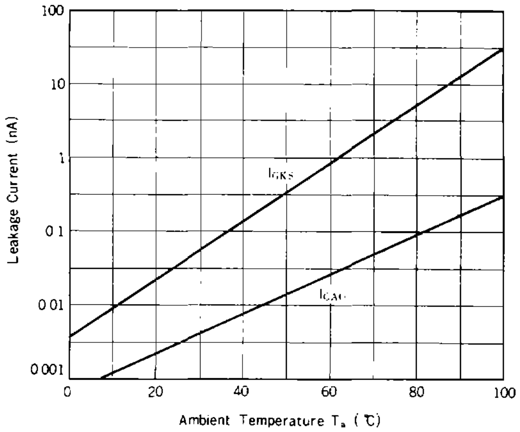

Fig. 13 I_{TRM}–P・W Maximum Rating

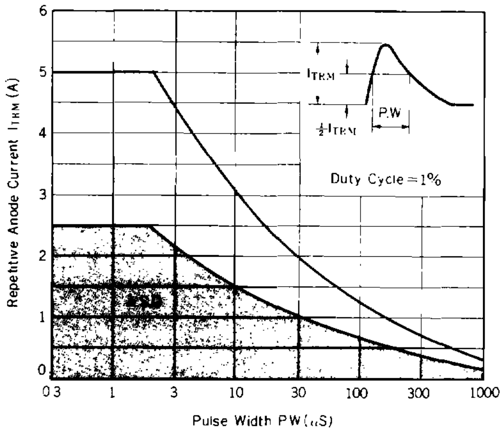

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Fig. 14 V_O–C–V Typical Characteristic

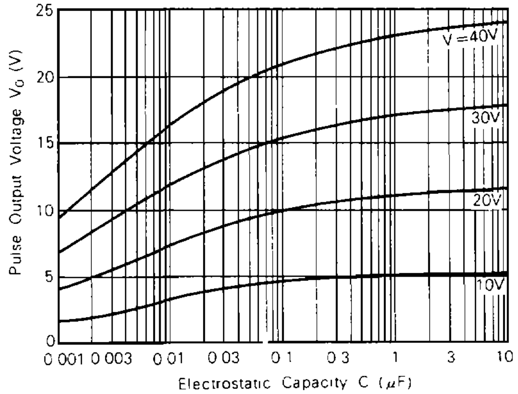


Fig. 15 V_O–V–C Typical Rating

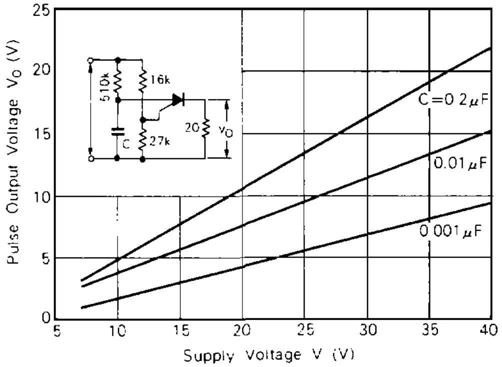


Fig. 16 Derating Wave

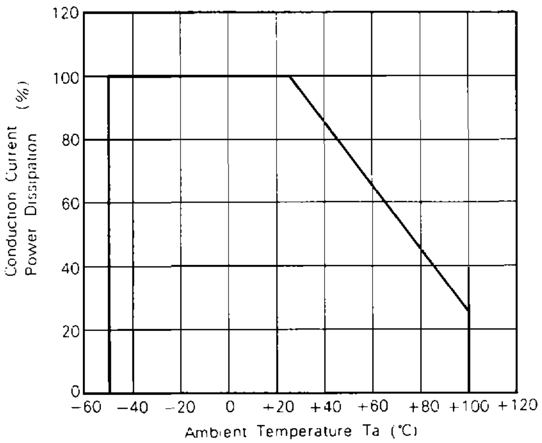


Fig. 17 I_F–V_F Typical Characteristic

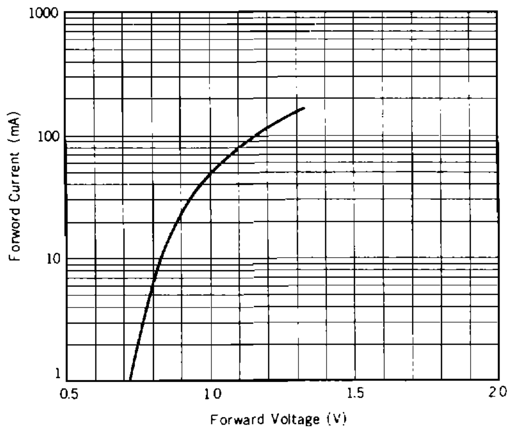
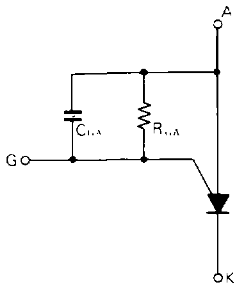


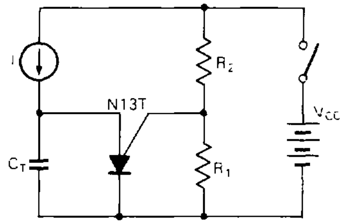
Fig. 18



When the N13T1 is used as a N-gate "SCR" Connect C_{GA} and R_{GA} as Fig. 18 shows.

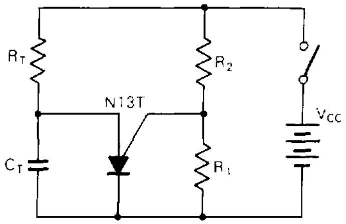
R_{GA}	C_{GA}
less than 5kΩ	3300pF
less than 10kΩ	4700pF

Approximate Design Equations for Timer



$$\tau = \frac{C_T}{I} \cdot V_P$$

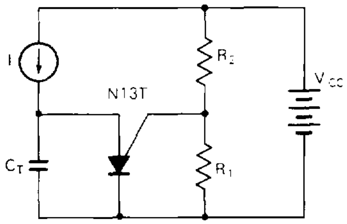
$$\begin{cases} V_P = \dfrac{R_1}{R_1 + R_2} \cdot V_{CC} + V_T \\ I_{C(leak)} + I_P \ll I \end{cases}$$



$$\tau = C_T \cdot R_T \ln \frac{1}{1 - \dfrac{\eta V_{CC} + V_T}{V_{CC}}}$$

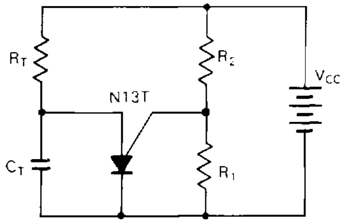
$$\begin{cases} \eta = \dfrac{R_1}{R_1 + R_2} \\ I_{C(leak)} + I_P \ll \dfrac{V_{CC} - V_P}{R_T} \end{cases}$$

Approximate Design Equations for Relaxation Oscillator circuit



$$T = \frac{C_T}{I} \cdot (V_P - V_V)$$

$$\begin{cases} V_P = \dfrac{R_1}{R_1 + R_2} \cdot V_{CC} + V_T \\ I_{C(leak)} + I_P \ll I \\ I < I_V \end{cases}$$



$$T = C_T \cdot R_T \ln \frac{1}{1 - \dfrac{\eta V_{CC} + V_T - V_V}{V_{CC} - V_V}}$$

$$\begin{cases} \eta = \dfrac{R_1}{R_1 + R_2} \\ I_{C(leak)} + I_P \ll \dfrac{V_{CC} - V_P}{R_T} \\ \dfrac{V_{CC} - V_V}{R_T} < I_V \end{cases}$$